EF1008-0

Datasheet

SCLO400-DRC001 July 2024

Quad Core Charge to Voltage Amplifier

FEATURES

- Input Capacitance: 1nF to 10nF
- Sensitivity: 1mV/pC
- Output Dynamic Range: up to ±4.8V_{Peak}
- Non-Linearity: ≤ 0.5%
- PGA: 1 to 32 in Binary Steps
- DC Level Adjustment: 0V, 1.25V, 1.65V, 2.5V
- Bandwidth: $f_{CL\,(3dB)}$ ≤5Hz, $f_{CH\,(3dB)}$ ≥120KkHz
- Analog Supply: ±5V, REF:+2.5V
- Digital Supply: +3.3V
- Power Dissipation: ≤ 350mW
- ESD up to ±2kV HBM (TBD)
- Package: 64 pin CQFP
- Temperature Range: -55ºC to +85ºC
- θ_{JC}:3.7°C/W

APPLICATIONS

- Shock and Vibration Transducers
- Acoustic Transducers
- Capacitive Sensors

DESCRIPTION

Charge to Voltage (C2V) Amplifier is a signal conditioning IC which conditions signal from vibration, shock and acoustic transducers. EF1008-0 consists of four programmable C2V Amplifier cores. The first stage is a C2V converter that produces output voltage proportional to the injected input charge. Output of C2V converter is followed by programmable gain amplifier (PGA) which pro six gain settings from 1 to 32 in binary steps and then PGA output is fed to a level shifter which changes the dc level of the final output.

Each core can be configured independently using input control pins. User can select any core by selecting control pins CH1 and CH0 and then setting gain of that particular core by applying appropriate value at the control pins PGA2, PGA1 and PGA0 and similarly the user can set dc levels of output by applying appropriate value at the control pins LS1 and LS0.

The device has two operating modes: transparent mode and latched mode. Suitable mode can be selected by appropriate value at ENABLE pin. In latched mode output will not respond to change of value at control pins.

BLOCK DIAGRAM

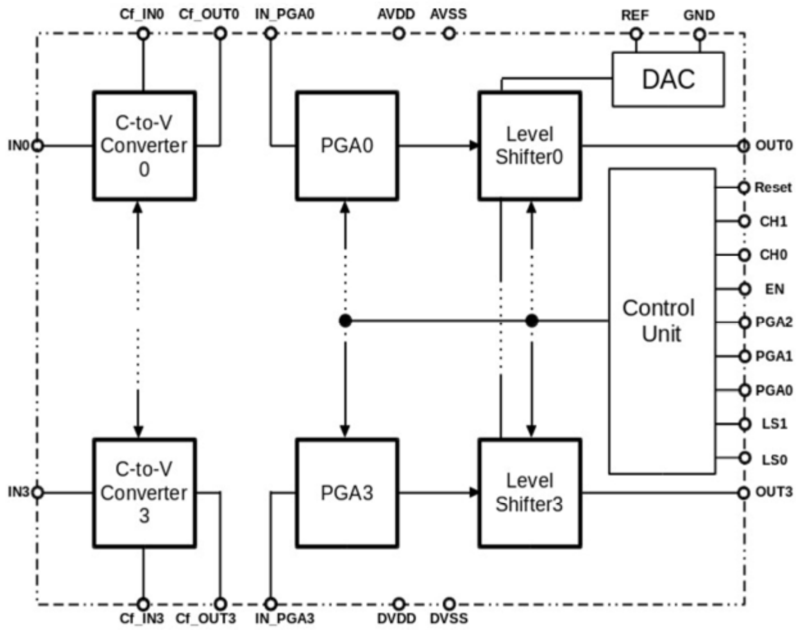

Figure-1: Block Diagram

PIN CONFIGURATION

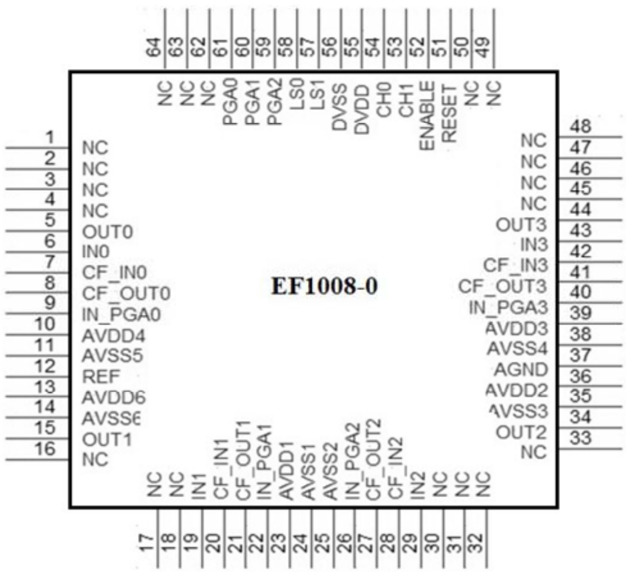

Figure-2: Device Pin Diagram

PIN DESCRIPTION

Table-1: Pin Description of EF1008-0

Pin No.	Name	Description/Remarks
1-4	NC	No Connection
5	OUT0	Core 0 Output
6	IN0	Core 0 Input
7	CF_IN0	Connect a feedback capacitor of value 1nF to 10nF between CF_IN0 and CF_OUT0
8	CF_OUT0	
9	IN_PGA0	Connect a coupling capacitor between IN_PGA0 and CF_OUT0
10	AVDD4	Analog Supply (+5V)
11	AVSS4	Analog Supply (-5V)
12	REF	External Reference Voltage (+2.5V). A current of V_{REF}/12K will flow from this pin
13	AVDD5	Analog Supply (+5V)
14	AVSS6	Analog Supply (-5V)
15	OUT1	Core 1 Output
16-18	NC	No Connection
19	IN1	Core 1 Input
20	CF_IN1	Connect a feedback capacitor of value 1nF to 10nF between CF_IN1 and CF_OUT1
21	CF_OUT1	
22	IN_PGA1	Connect a coupling capacitor between IN_PGA1 and CF_OUT1
23	AVDD1	Analog Supply (+5V)
24	AVSS1	Analog Supply (-5V)
25	AVSS2	Analog Supply (-5V)
26	IN_PGA2	Connect a coupling capacitor between IN_PGA2 and CF_OUT2
27	CF_OUT2	Connect a feedback capacitor of value 1nF to 10nF between CF_IN2 and CF_OUT2
28	CF_IN2	
29	IN2	Core 2 Input
30-33	NC	No Connection
34	OUT2	Core 2 Output
35	AVSS3	Analog Supply (-5V)
36	AVDD2	Analog Supply (+5V)
37	AGND	Analog Ground (0V)
38	AVSS4	Analog Supply (-5V)

Pin No.	Name	Description/ Remarks
39	AVDD3	Analog Supply (5V)
40	IN_PGA3	Connect a coupling capacitor between IN_PGA3 and CF_OUT3
41	CF_OUT3	Connector a feedback capacitor of value 1nF to 10nF between CF_IN3 and CF_OUT3
42	CF_IN3	
43	IN3	Core 3 Input
44	OUT3	Core 3 Output
45-50	NC	No Connection
51	RESET	Active Low Reset
52	ENABLE	Transparent Mode / Latch Mode Enable Bit
53	CH1	Core Selection Pin: Bit 1
54	CH0	Core Selection Pin: Bit 0
55	DVDD	Digital Supply (3.3V)
56	DVSS	Digital Ground (0 V)
57	LS1	Control Bit1 for Output DC Level
58	LS0	Control Bit 0 for Output DC Level
59	PGA2	Control Pin for PGA Setting Pin: Bit 2
60	PGA1	Control Pin for PGA Setting Pin: Bit 1
61	PGA0	Control Pin for PGA Setting Pin: Bit 0
62-64	NC	No Connection

ABSOLUTE MAXIMUM RATING

Table-2: Absolute Maximum Rating

AVDD	+6 V
AVSS	-6 V
AGND	-0.3 to 0 V
DVDD to DVSS	-0.3V to +4.2V
Analog Input Level	(AVSS-0.3V) to (AVDD+0.3V)
Digital Input Level	-0.3V to (DVDD+0.3V)
Storage Temperature	-60 ºC to +125 ºC

RECOMMENDED OPERATING CONDITIONS

Table-3: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
AVDD	Analog Positive Supply	4.5	5	5.5	V
AVSS	Analog Negative Supply	-5.5	-5	-4.5	V
DVDD	Digital Power Supply	3.0	3.3	3.6	
V_{IH}	High Level Input Voltage	2.4	-	DVDD	V
V_{IL}	Low Level Input Voltage	DVSS	-	0.8	V
T_A	Ambient Temperature Range	-55	-	+85	ºC

ELECTRICAL CHARACTERISTICS

All specifications are at AVDD = 5V, AVSS = -5V, DVDD =3.3V, REF = 2.5V, C_{IN}=C_F=1nF, R_F=50 MΩ, PGA=1 and Temperature= -55°C to 85°C, unless otherwise specified.

Table-4: Electrical characteristics of EF1008-0

PARAMETER	TEST CONDITION	EF1008-0			UNIT
		MIN	TYP	MAX	
ANALOG PERFORMANCE					
Analog Input Current				75	µA
Programmable Gain Amplifier	User Selectable	1		32	
Scale Factor				1	mV/pC
Maximum Dynamic Output	Gain =1	-4.40		4.80	Vpeak
	Gain≥2	-4.80		4.80	Vpeak
Frequency Response:					
Low Cutoff $f_{CL\,(3DB)}$	Low Cutoff $f_{CL\,(3DB)}$	3.5	4	4.5	Hz
High Cutoff $f_{CH\,(3DB)}$	High Cutoff $f_{CH\,(3DB)}$	120	133	150	KHz
Roll-off rate	1.2 f_{CH} to 2.4 f_{CH}	4		9	dB
Pass Band Error	50Hz to 20KHz			1.5	%
DC Level (DC Bias) Error	F_{IN}≤10KHz, LS1:LS0 = 0, 1, 2 & 3			±50	mV
DC Bias Stability	AVDD, AVSS Variation :±10%			±50	mV
DC Bias Drift	-55°C to 85°C, Box Method			±0.5	mV/°C
Full Scale Output (FSO) Error	F_{IN} = 110Hz, 1KHz, 10KHz			±1	%
FSO Stability	AVDD, AVSS Variation :±10%			±0.5	%
FSO Drift	-55°C to 85°C, Box Method			50	ppm FSO /°C
Scale Factor Error	F_{IN} = 110Hz, 1KHz, 10KHz			±1	%
Scale Factor Stability	AVDD, AVSS Variation :±10%			±0.5	%
Scale Factor Drift	-55°C to 85°C, Box Method			50	ppm /°C
Non- Linearity	Best fit Method			0.5	%FSO
Output Impedance			10	20	Ω
EXTERNAL REFERENCE					
REF	2.5V			0.5	mA
POWER SUPPLY REQUIREMENT					
Analog Supply Current	AVDD: 5V±10%		35.0	50	mA
	AVSS: -5V±10%	-50	-35.0		mA
Digital Supply Current	DVDD: 3.3V±10%		0.01	1	µA
TEMPERATURE RANGE					
Operating		-55		85	°C

TYPICAL CURVES

All specifications are at AVDD = 5V, AVSS = -5V, DVDD =3.3V, REF = 2.5V, C_{IN}=C_F=1nF, R_F=50 MΩ, PGA=1 and Temperature= 25°C, unless otherwise specified.

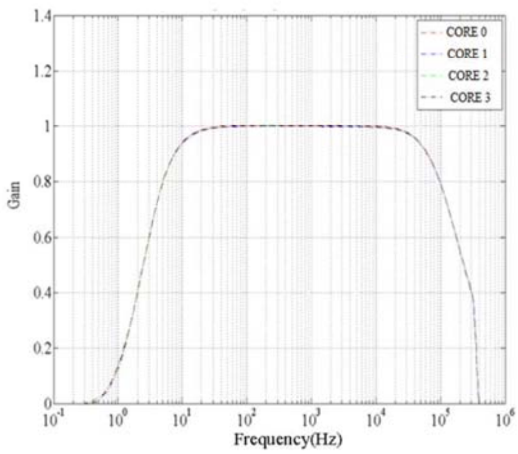

Figure-3: Frequency-Response

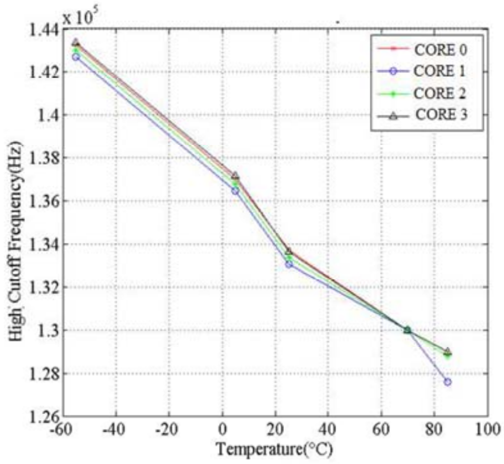

Figure-4: f_{CH} (3dB) vs. Temperature

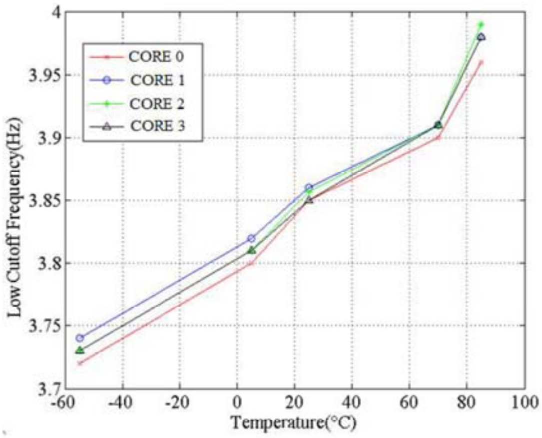

Figure-5: f_{LH} (3dB) vs. Temperature

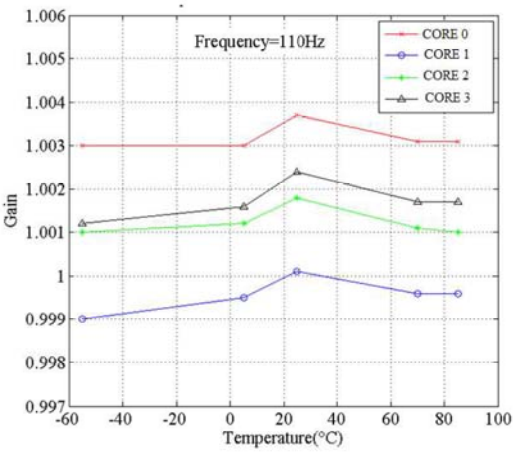

Figure-6: Scale-Factor vs. Temperature

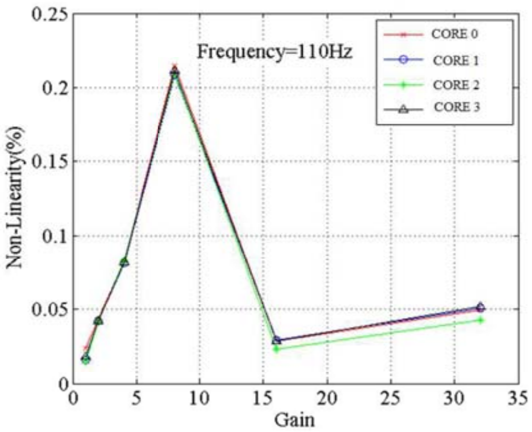

Figure-7: Non-Linearity vs. PGA

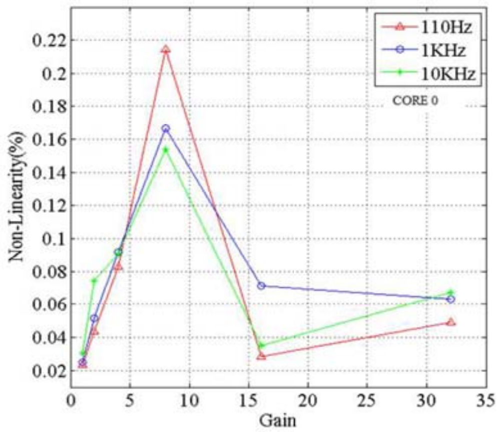

Figure-8: Non Linearity vs. PGA

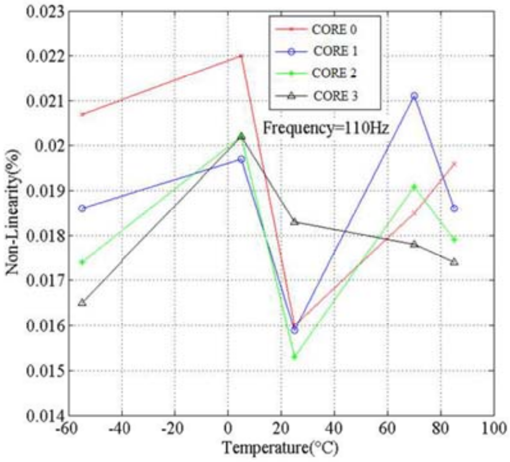

Figure-9: Non Linearity vs. Temperature

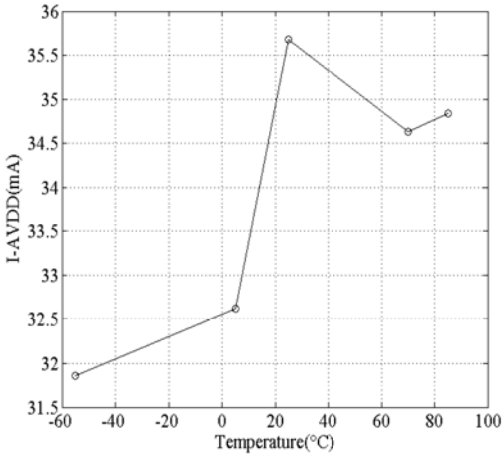

Figure-10: I_{AVDD} vs. Temperature

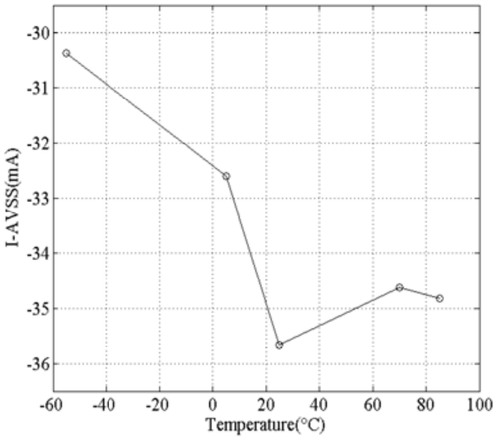

Figure-11: I_{AVSS} vs. Temperature

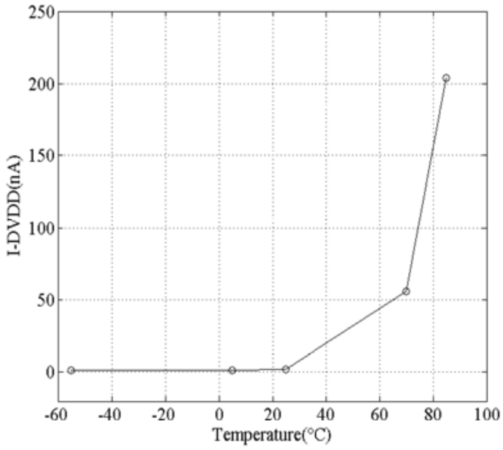

Figure-12: I_{DVDD} vs. Temperature

DEVICE OVERVIEW

C2V CONVERTER

This is a primary block which converts charge into voltage with a gain of $1/C_f$. A feedback Capacitor C_f is to be connected externally between CF_IN and CF_OUT pins. Value of C_f can vary between 1nf and 10nf.

The C2V converter offsets input current with the feedback capacitor and produces output voltage inversely proportional to the feedback capacitor but proportional to total input charge flowing through the specified time.

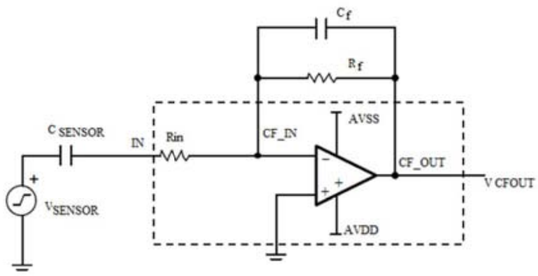

Figure-13: C2V Converter

$$V_{CFOUT} = Q_{in}/C_F \quad \text{[Eq-1]}$$

Where Qin = $C_{SESNOR}*V_{SENSOR}$. The resistor R_f is to be connected externally to provide the DC operating point for op-amp. Its value must be high to minimize the noise impact and higher than the impedance of C_f at lowest frequency of interest. Select 50MΩ value for resistor R_f.

CORE SELECTION

EF1008-0 consists of four cores of C2V amplifier. All cores work in parallel. User can program PGA value and DC level of any core. The core to be programmed can be selected using CH1 and CH0 pins.

Table-5 Core Selection Control Settings

Sr. No.	CH1:CH0	Selected Core
1	00	Core 0
2	01	Core 1
3	10	Core 2
4	11	Core 3

PGA

There are separate PGA blocks for each C2V amplifier core. Output of the C2V converter goes into PGA block through a coupling capacitor. The coupling capacitor of value 1µF should be connected between CF_OUT and IN_PGA pins. PGA block has 6 different gains setting from 1 to 32 in binary steps. These gains can be programmed using control pins PGA2, PGA1 and PGA0.

Table-6: PGA Control Settings

Sr. No.	PGA[2: 0]	Gain
1	000	1
2	001	2
3	010	4
4	011	8
5	100	16
6	101	32

Note: PGA 2 will be selected in case user set PGA2:PGA0 as 110 or 111.

LEVEL SHIFTER

The output of PGA block directly goes to level shifter block. Level shifter block provides an option to shift the DC voltage level of the output. There are four different DC levels: 0V, 1.25V, 1.65V and 2.5V.These levels can be selected by control pins LS1 and LS0.

Table-7: Level Shifter Control Settings

Sr. No.	LS1: LS0	Output DC level (V)
1	00	0
2	01	1.25
3	10	1.65
4	11	2.5

PROGRAMMING

User can change PGA and output DC level of any core by selecting CH1:CH0 bits and by applying appropriate input control signals (PGA, LS and ENABLE). There are two modes of operation in EF1008-0: Transparent Mode and Latched Mode. Any of the modes can be selected by applying appropriate signal at the ENABLE pin.

I. TRANSPARENT MODE

This mode will be selected when ENABLE = 0. In this mode, the device output will directly respond to the change in the values of the control signals (PGA and LS).

II. LATCHED MODE

This mode will be selected when ENABLE = 1. In this mode, the PGA and DC level values set for a particular channel will be latched.

Figure 3 shows the timing diagram to put the core into latch mode. Use the following procedure for latch mode.

- Select Core with control pins CH1:CH0.
- Set PGA by applying appropriate level at PGA2:PGA0 pins.
- Set DC Level by applying appropriate level at LS1:LS0 pins.
- Set ENABLE=0 device will be in transparent mode. During this mode PGA and DC level of selected core will be set.
- Set ENABLE = 1 to latch the set value of PGA and output dc Level.
- Repeat above steps to set PGA and output dc level of another core.

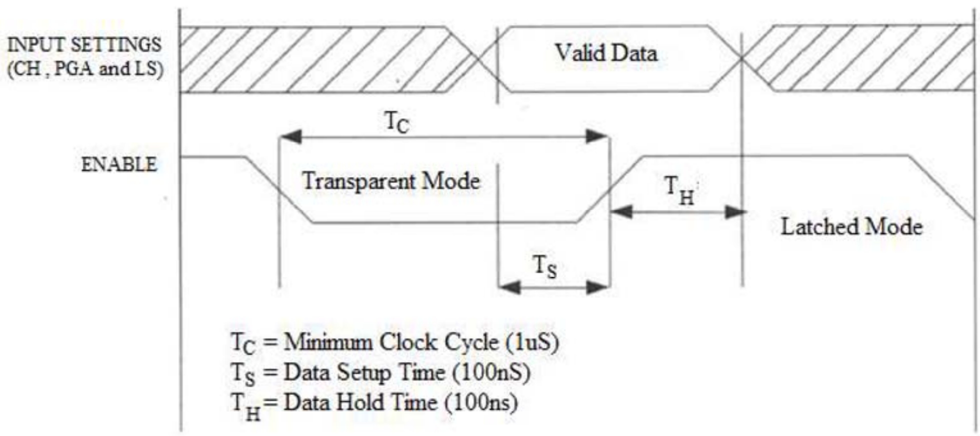

Figure-14: Timing diagram to put the device core into latch mode

PACKAGE INFORMATION

64-Pins CQFP

All dimensions are in mm unless specified otherwise.

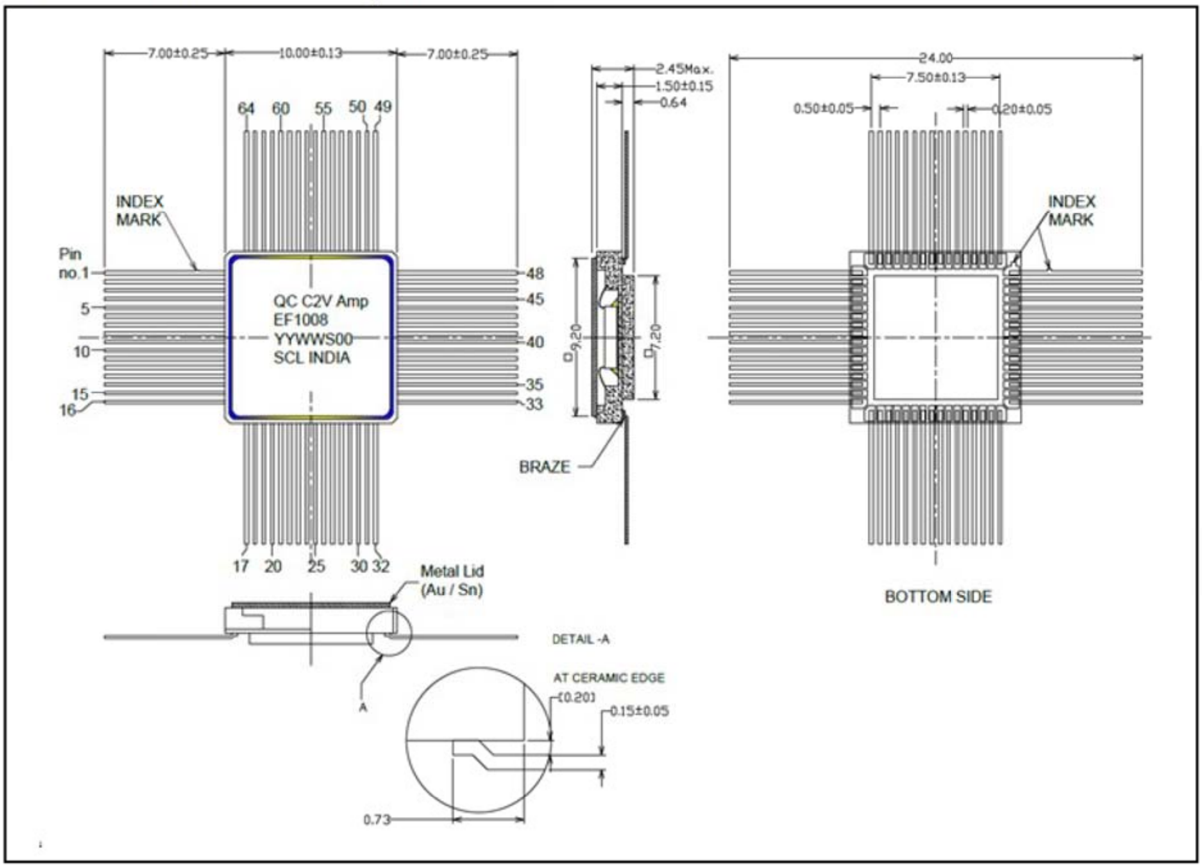

Figure-15: Package Drawing

REVISION HISTORY

Table-8: Revision History

S. No.	Version	Date of release	Description
1	SCLO400-DRC001	July 2024	First Release

DISCLAIMER

Standard SCL legal terms and conditions applicable.