

# **EVALUATION BOARD V1.0**

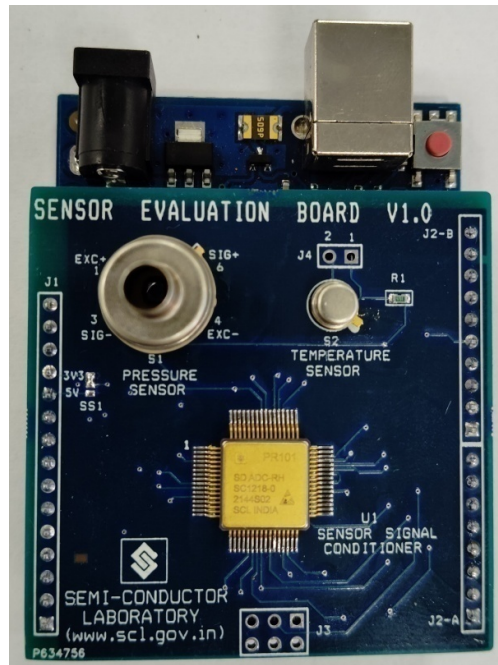
**For**

**Pressure Sensor**

**Temperature Sensor**

**& Readout IC SC1218**

## **User Operational Manual**



**MEMS Test & Application Development Division**

**Electronics Fabrication & Test Group**

**Semi-Conductor Laboratory**

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S. No.	Title	Page
1	Introduction	3
2	Evaluation Board Kit Details	4
3	Evaluation Board Operational Guide	5
4	Hardware Description	6-10
5	Evaluation Board Schematic	11
6	Evaluation Board Layout	12
7	Pressure Sensor Calibration & Compensation	13
8	Temperature Sensor Calibration	14
Annexure-A: Pressure Sensor Datasheet		15-16
Annexure-B: Temperature Sensor Datasheet		17-21
Annexure-C: Readout IC SC1218 Datasheet		22-43

## **1. Introduction**

1. EV Board is aimed to evaluate following components:
  - SCL Temperature Sensor (PRT)
  - SCL Pressure Sensor (1.5 Bar)
  - SCL Readout ASIC SC1218
2. EV Board provides corrected Pressure (mBar) & Temperature (°C) readings. Sensor calibration coefficients and ASIC (SC128) configuration registers are programmed for SCL sensors mounted on the board.
3. Sensors & readout ASIC (SC1218) are soldered for contact reliability. User may de-solder Pressure & Temperature sensors from EV board to replace their own sensors to evaluation by using SC1218.
4. After removing SCL Sensors, user needs to calibrate/compensate their Pressure & Temperature Sensors and re program readout ASIC (SC1218) for their sensor values.
5. EV Board comes with pre programmed calibration coefficient for SCL sensors. A paper sheet also provided with listing of calibration coefficients pre programmed. User may any time restore factory settings by placing SCL sensors & entering default calibration coefficients into EV Board.
6. EV Board is developed compatible with Arduino UNO R3 boards. Arduino boards are very popular among students, low in cost & readily available in local market. Arduino programming IDE is free to download & provides user friendly programming platform.
7. Students can download Arduino IDE software from website:
8. Students can download Arduino compatible firmware of EV Board from SCL website. Students may edit firmware & write their own calibration algorithms for their sensor development.
9. Student will connect EV Board to PC through compatible USB cable, open EV board firmware into Arduino IDE platform.
10. EV board is programmed with sensor coefficients also mentioned in calibration sheet provided with EV Board KIT. Before reprogramming the EV board, student has to enter calibration coefficients comes with EV Board KIT into firmware.
11. Student can download Reference User Manual from SCL website. Manual contains quick start guidelines, details of EV Board Hardware & Software and Component datasheet for ready reference.

## 2. EV Board Kit Details

S.No.	Hardware Description	
1	Sensor Evaluation Board V1.0 Assembled Board with following parts designed & developed by SCL	
	1a	Pressure Sensor (S1)
	1b	Temperature Sensor (S2)
	1c	Sensor Signal Conditioner (U1)
	1d	Mounting Connectors compatible with Arduino UNO board J1 & J2 (J2-A & J2-B)
2	Arduino UNO R3 Board (Optional)	
3	USB interface data Cable (Optional)	

S.No.	Download Links	
1	<b>Arduino UNO Support Files</b> Install latest version of Arduino IDE (Arduino IDE 2.2.1) on your PC.	<a href="https://www.arduino.cc/en/software">https://www.arduino.cc/en/software</a>
2	<b>Sensor Readout Code</b> Download Sensor Readout Software code. Open & Run in Arduino IDE 2.2.1	<a href="https://www.scl.gov.in">https://www.scl.gov.in</a>
3	<b>Evaluation Board User Manual</b> Download Operational User's Manual which contains: <ul style="list-style-type: none"> <li>• installation guidelines</li> <li>• Interface &amp; Operation details</li> <li>• Sensor &amp; IC datasheets</li> <li>• Schematics &amp; PCB layout</li> </ul>	<a href="https://www.scl.gov.in">https://www.scl.gov.in</a>

### **3. Evaluation Board Operational Guide:**

Use the following procedure to operate the sensor evaluation kit:

1. Install the latest version of Arduino Uno IDE (Arduino IDE 2.2.1) on your PC/Laptop.
2. Download the Sensor Readout Software code from SCL website using the link mentioned in instruction sheet available with this kit.
3. Connect the evaluation board using USB cable to your PC/Laptop.
4. Open the sensor readout software. Enter the calibration and compensation coefficients for pressure sensor ( $A_1$  to  $A_6$ ) and temperature sensor (A, B) in the code.
5. Run the code in Arduino IDE 2.2.1.
6. The output corresponding to input pressure and input temperature will be displayed in mBar and degree C on serial monitor of Arduino on your PC/Laptop.
7. You may change the input pressure and temperature, run the Arduino code and check the corresponding output on serial monitor.
8. If you want to use sensors other than the ones provided with this kit, you may remove the SCL make sensor and assemble your sensors, in TO-8 header for Pressure sensor & TO-46 header for temperature sensor (a provision of two pins is also provided along with TO-46 header for temperature sensor. If you want to use temperature sensor assembled in a package with two pin footprint, you may use this option) on the PCB provided to you, enter the compensation and calibration coefficients of your sensors, run the Arduino code and verify the output.

#### **Required Equipments:**

1. PC/Laptop
2. Sensor Pressure source
3. Sensor temperature source

#### **Sensor Evaluation kit contents:**

The kit comes with calibrated and compensated pressure and temperature sensors mounted on a PCB along with ADC (SC1218). Temperature compensation is done in range of 10°C to 50°C.

Material included in the kit is given below:

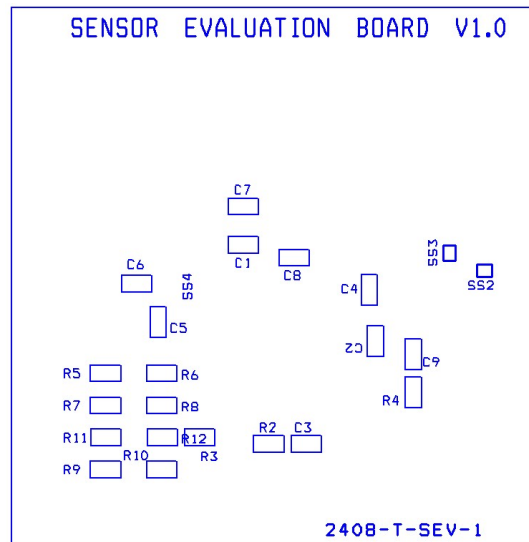
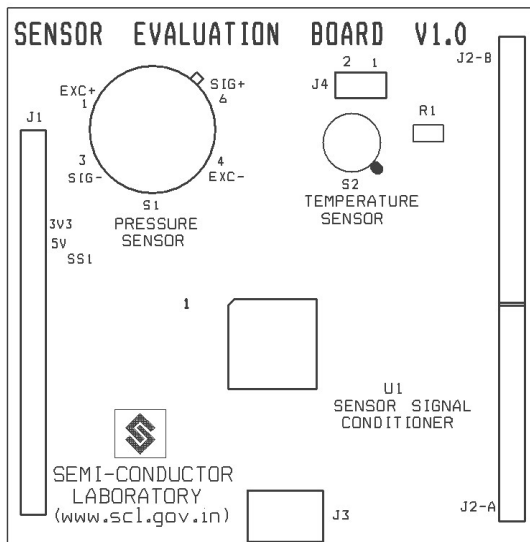
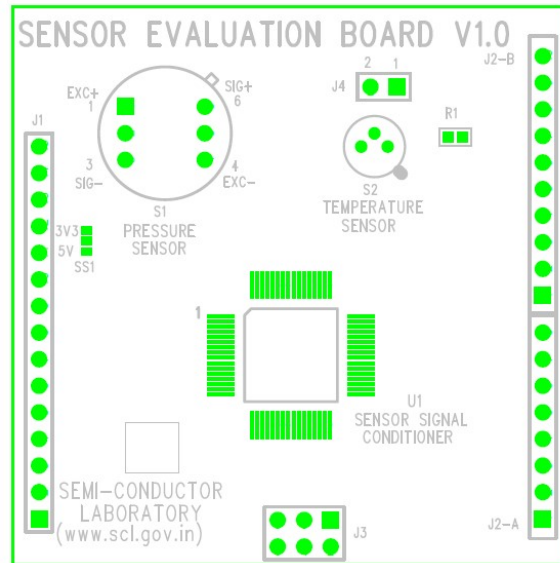
1. Evaluation board with compensated sensors and Arduino Uno.
2. USB cable

Instruction sheet containing the compensation coefficients of both the sensors

## 4. Hardware Description

EV Board provides corrected Pressure (mBar) & Temperature ( $^{\circ}\text{C}$ ) readings. Sensor calibration coefficients and ASIC (SC128) configuration registers are programmed for SCL sensors mounted on the board.

Kit includes an assembled Sensor Evaluation Board V1.0 Major components mounted are pressure sensor, temperature sensor and readout IC SC1218. Sensor Evaluation Board V1.0 is pin compatible with Arduino Uno R3 board for interface & display at PC through USB cable.



## Component List

Reference	Quantity	Description
S1	1	Pressure Sensor (TO-8)
S2	1	Temperature sensor (TO-46)
U1	1	Readout IC, SC1218-0 (CQFP-64)
<b>Jumpers/Connectors &amp; Solder Select</b>		
J1	1	CON15; Power Connector
J2-A	1	CON8; Arduino Digital 8-Pin Connector (DRDY signal)
J2-B	1	CON10; Arduino Digital 10-Pin Connector (SPI signals)
J3	1	CON3X2;
J4	1	CON2; Unused, alternate sensor site
SS4	1	Solder Short
SS1, SS2, SS3	3	Solder Short
<b>Other Passive Components</b>		
C <sub>1</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>9</sub>	6	0.1μF ceramic X7R capacitors
C <sub>2</sub>	1	1μF ceramic X7R capacitors
C <sub>7</sub> , C <sub>8</sub>	2	1KpF ceramic X7R capacitors
C <sub>9</sub>	1	0.1μF ceramic X7R capacitors
R <sub>1</sub> , R <sub>2</sub>	2	4.75KΩ Resistor
R <sub>3</sub> , R <sub>4</sub> , R <sub>5</sub> , R <sub>7</sub> , R <sub>9</sub> , R <sub>11</sub>	6	1KΩ Resistor
R <sub>6</sub> , R <sub>8</sub> , R <sub>10</sub> , R <sub>12</sub>	4	2KΩ Resistor

### Pressure Sensor (S1)

Pressure sensor (S1), packaged in 6-pin TO-8 package is mounted on top side. SCL pressure sensor is piezo resistive wheat stone bridge with four (04) active elements. Bridge resistance of sensor is ~2KΩ. Pressure sensor is exited with reference voltage 1.22V by using REFOUT signal of SC1218. Sensor output signal (INP2 & INN2) corresponds to measured pressure is connected to channel-2 of SC1218.

Datasheet of Pressure sensor is in annexure-A

### Temperature Sensor (S2)

Temperature sensor (S2), packaged in 3-pin TO-46 package is also mounted on top side. SCL temperature sensor is Pt based thin film PRT. Sensor nominal resistance at 25°C is 1 KΩ. Temperature sensor is exited with reference voltage 1.22V by using REFOUT signal of SC1218. A series Current limiting resistor R1 (4.75KΩ) is connected to limit the current through PRT (~ 0.2mA). Sensor output signal (INP1) corresponds to measured temperature is connected to channel-1 of SC1218.

Datasheet of Temperature sensor is in annexure-B

## SC1218 (U1)

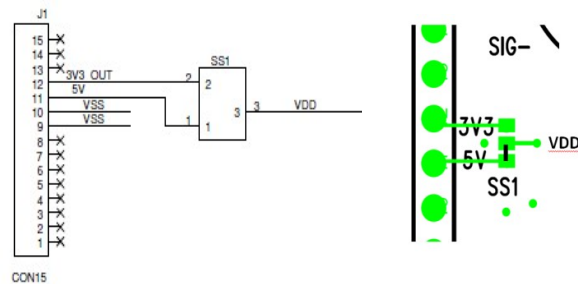
SC1218 (U1) is SCL developed sensor readout IC with 24-bit sigma delta ADC. SC1218 is packaged in CQFP-64 package and mounted on top side of evaluation board.

Datasheet of SC1218 is in annexure-C

Analog outputs of both pressure & temperature sensors are fed to two different channels of SC1218. SC1218 provides gain & produce 24-bit digital data on SPI bus. An SPI master (Ardiuno Uno in this case) will read the pressure and temperature data on SPI bus and the same will be displayed on serial monitor of Ardiuno IDE on PC/Laptop.

## Power Connector (J1)

SC1218 operates at 3.3V. Evaluation board supply voltage VDD is shorted with 3.3V output from Ardiuno Board as shown below:



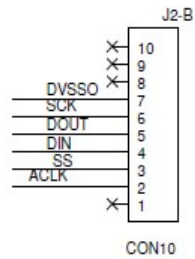
Pin	Signal	Description	Pin	Signal	Description
1	NC	-	9	VSS	GND
2	NC	-	10	VSS	GND
3	NC	-	11	5V	Power Supply
4	NC	-	12	3.3V	Power Supply
5	NC	-	13	NC	-
6	NC	-	14	NC	-
7	NC	-	15	NC	-
8	NC	-			



## Signal Connector (J2)

### J2-A connector

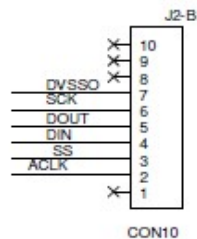
Figure below shows the schematic part corresponding to J2-A connector.



Pin	Signal	Description	Pin	Signal	Description
1	NC	-	5	NC	-
2	NC	-	6	NC	-
3	NC	-	7	DRDY	Data Ready Signal, (active low)
4	NC	-	8	NC	-

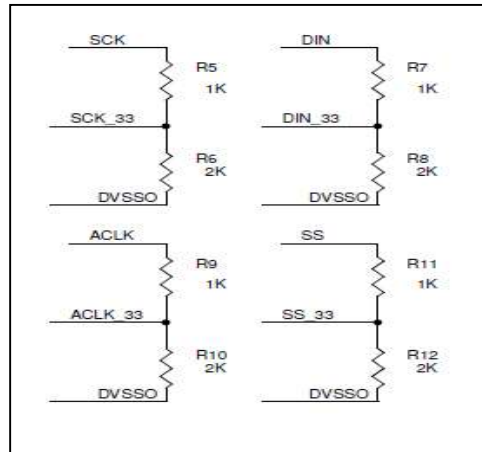
(DRDY) Data Ready is active Low Signal. The DRDY pin is used as a status signal to indicate when new digital code is ready to be read from the ADC. DRDY goes low when new data is available. It becomes high when a read operation from the data register is executed using RDATA or RDATAAC command. The DRDY pin goes high at the middle of read of 2nd MSB byte. In case, when no read operation is performed, DRDY will remain low. After switching channel (for reading pressure or temperature) wait for three DRDY active low cycles before reading the data of the switched channel.

### J2-B connector

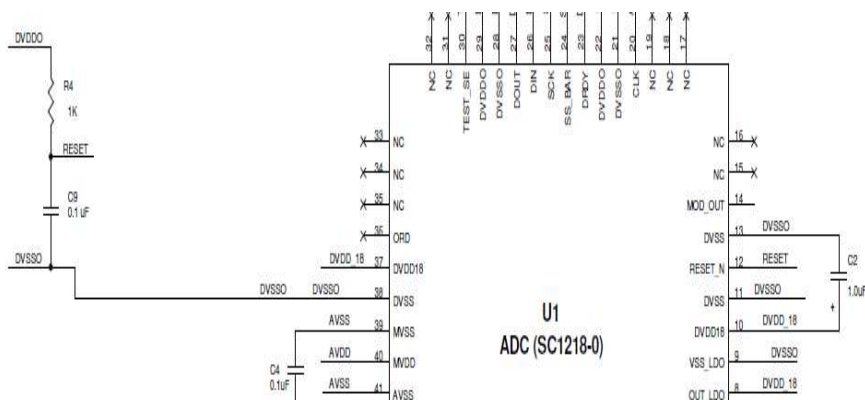


Pin	Signal	Description	Pin	Signal	Description
1	NC	-	6	SCK	Serial Clock
2	ACLK	ADC Clock Input	7	DVSSO	GND
3	SS	Serial Interface Enable, active low	8	NC	-
4	DIN	Serial Data In	9	NC	-
5	DOUT	Serial Data Out	10	NC	-

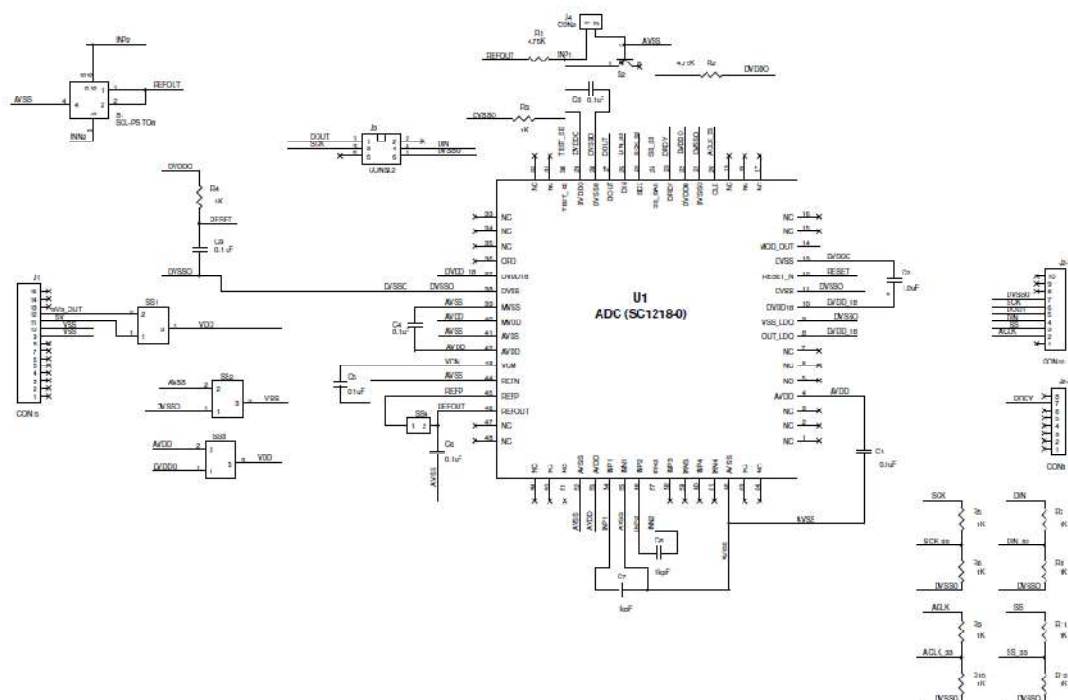
Arduino Uno works for 5V supply and generates SPI signals of 5V level, whereas SC1218 is operated with a supply of 3.3V and it generates 3.3V signals. Therefore level translators (5V to 3.3V) are incorporated in the evaluation board. Figure below shows the potential divider circuit part of schematic which is used as level translator.



A power on reset RC circuit is implemented for SC1218. Details is shared in datasheet of SC1218.

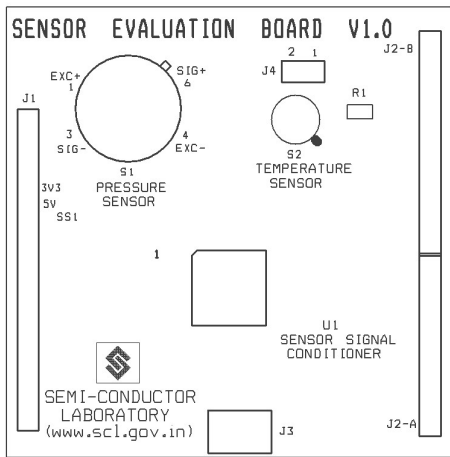


## 5. Evaluation Board Schematic

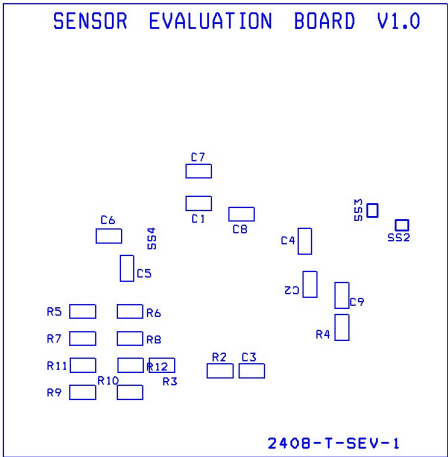


### EV Board Schematic Diagram

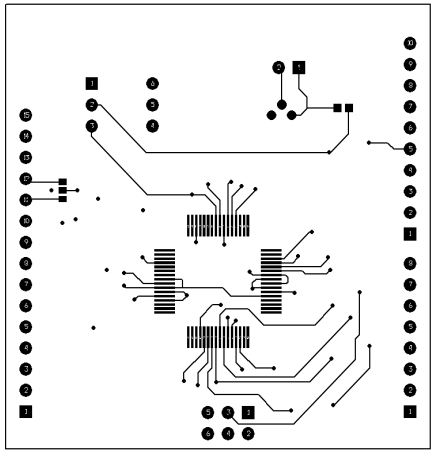
## 6. Evaluation Board Layout



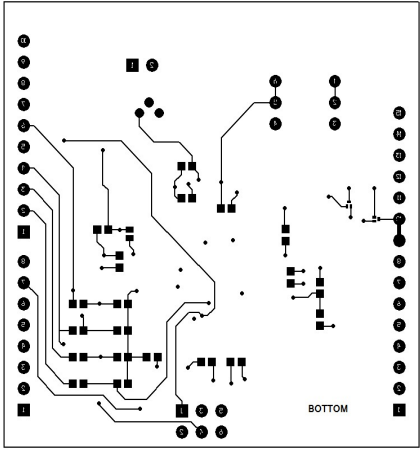
Silk Screen Top



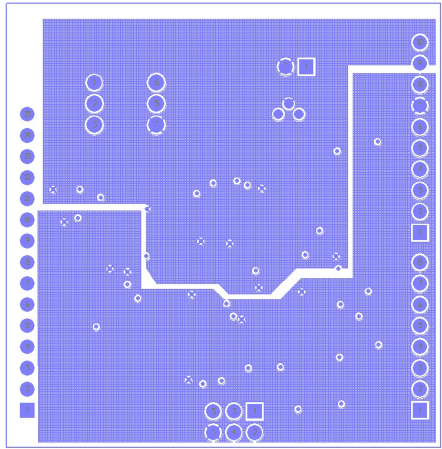
Silk Screen Bottom



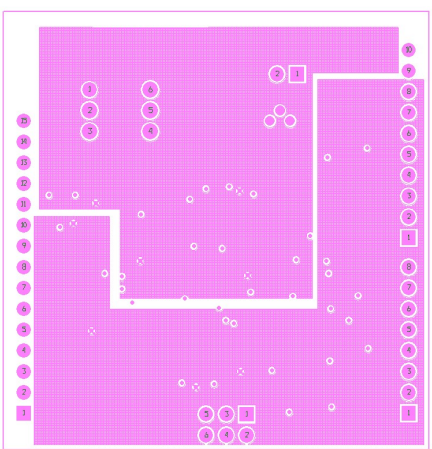
Top Layer



Bottom Layer



Inner 1 (VSS)



Inner 2 (VDD)

## 7. Pressure Sensor Calibration & Compensation

Pressure sensor is in the form of a close Wheatstone bridge. Bridge is excited by on-chip (REFOUT of SC1218) generated 1.22V. REFOUT is also used for ADC reference. Differential output of pressure sensor is then amplified by PGA of 128. Amplified sensor output is then digitized by sigma delta ADC.

Table below shows the settings of SC1218 for pressure sensor:

Serial No.	Configuration Register	Value
1	PGA	128
2	OSR	256
3	CR1	0xE1
4	CR2	0x03

After configuration programming, raw data of pressure sensor was captured for input pressure (200mBar to 1500mBar) for temperature range of 10°C to 40°C and the output data was read from SC1218 through SPI.

Temperature compensation and calibration coefficients are computed for each sensor using following equation:

$$P \text{ (Calibrated)} = A_1 * P * T^2 + A_2 * P * T + A_3 * P + A_4 * T^2 + A_5 * T + A_6$$

Where:

P (Corrected) = Temperature Compensated & Calibrated Pressure Data in mbar

P = Raw Pressure digital data,

T = Raw Temperature digital data

A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub>, A<sub>4</sub>, A<sub>5</sub>, A<sub>6</sub> = Coefficients

These coefficients will be entered in the SPI read source code to get final corrected pressure value in mBar on serial monitor.

Coefficients corresponding to each sensor are provided with the sensor evaluation kit.

## 8. Temperature Sensor Calibration

Sensor output was captures for temperature range of 10°C to 40°C and the output data was read from SC1218 through SPI.

Table below shows the settings of SC1218 for temperature sensor:

Serial No.	Configuration Register	Value
1	PGA	4
2	OSR	64
3	CR1	0x40
4	CR2	0x05

The sensor is calibrated (range) and the calibration coefficients are computed for each sensor using following equation:

$$R_T = R_0 (1 + AT + BT^2)$$

$R_T$  = Resistance at Temperature  $T^{\circ}\text{C}$

$R_0$  = Resistance at Temperature  $0^{\circ}\text{C}$

$T$  = Raw Temperature digital values read through (SPI)

$A, B$  = Coefficients

These coefficients will be entered in the SPI read source code to get final corrected temperature value in degree C on serial monitor.



## Annexure-A: Pressure Sensor Datasheet



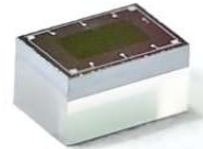
### PRODUCT DESCRIPTION:

SCL's MEMS based pressure sensors are in the form of Bridge of four piezo-resistors to give differential output proportional to applied pressure. The absolute sensors have an internal vacuum reference.

These are intended for use with Non-corrosive, Non-ionic working fluids; such as air and dry gases.

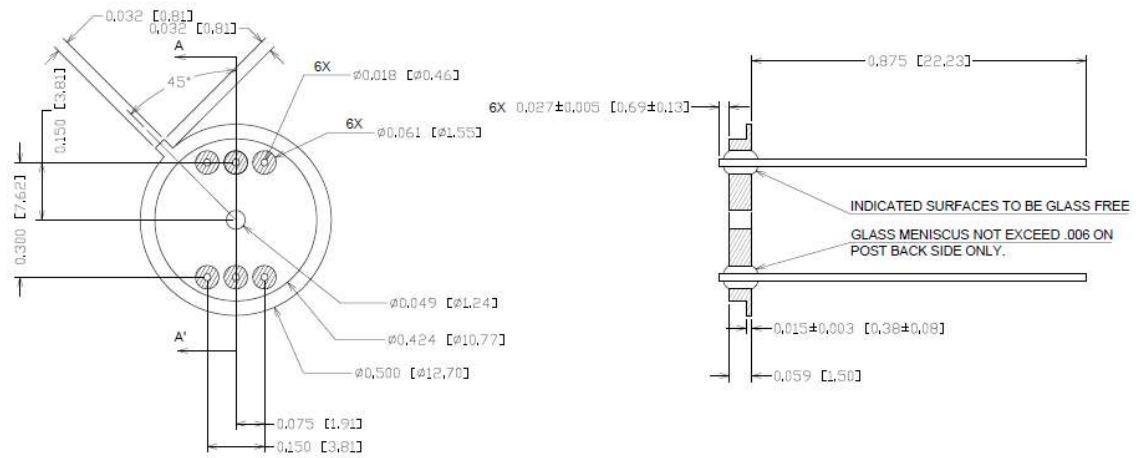
### FEATURES:

- Operating Ranges : Upto 30 bar
- Package : TO headers, PCB (COB)
- Custom Package option available
- Sensor dies are available

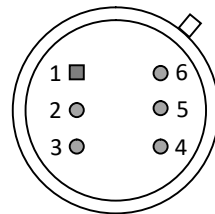


Product Specifications			
S.No.	Parameters		Specification
1	Operating Pressure Range		Upto 5 bar
2	Pressure Reference		Absolute
3	Proof Pressure		> 1.5 Times Operating Pressure
4	Burst Pressure		>3 Times Operating Pressure
5	Operating Temperature		-40°C to 125°C
6	Storage Temperature		-40°C to 125°C
7	Bridge Resistance (at 25°C)		3.0 KΩ ± 1 KΩ
8	Non-Linearity		<0.2 % FSR
9	Hysteresis		<0.1%FSR
10	Repeatability		<0.1%FSR
11	Bridge Voltage		3V (Typ.), 1V – 5V
12	Full Scale Range (FSR)		75 ± 25 mV (at 3Vexc)
13	Offset		±10 mV/V
14	TC of Bridge Resistance (TCR)		1000±250 (ppm/°C)
			2000±250 (ppm/°C)
15	TC of Span (TCS)	Voltage Excitation	-2000±500 (ppm/°C)
16	TC of Offset (TCO)		±25 uV/V/°C
17	Response Time		< 5ms

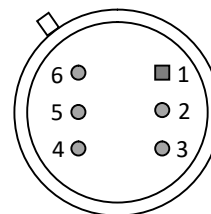
# HEADER



NOTE : All Units in inches [mm]



Top View



Pin View

Pin	Signal Name	Description
1	EXC+	Bridge Excitation Positive (Connected with VREFOUT = 1.22V of SC1218)
2		
3	SIG-	Differential Signal Negative Output
4	SIG+	Differential Signal Positive Output
5	EXC-	Bridge Excitation Negative (Connected with Ground)
6		





## Annexure-B: Temperature Sensor Datasheet



### PRODUCT DESCRIPTION:

Temperature sensors are thin film platinum based PRTs. Nominal resistance at ambient is around 1 K $\Omega$  with sensitivity of 3 $\Omega$ /°C.

Sensor variants with nominal resistance  $R_0$  values of 100 $\Omega$ , 500 $\Omega$  & 1500 $\Omega$  can also be customized as per application requirements.

### FEATURES:

- Operating Ranges : -20°C to 100°C
- Accuracy : 1°C
- Nominal Resistance ( 25°C ) : 1K $\Omega$   $\pm$  5%
- Sensitivity : 3 $\Omega$ /°C
- Package : TO-46/52, Bare Dies, Custom
- Die Size : 2.0 mm x 2.5 mm x 0.675 mm

Product Specification		
S.No.	Parameters	Specification
1	Temperature Range <sup>1</sup>	-20°C to 100 °C
2	Calibration Accuracy <sup>2</sup>	0.1°C
3	Nominal Resistance (at 0°C), $R_0$	900 $\Omega$
4	Nominal Temperature Coefficient, TCR	0.00315 $\Omega$ /°C
5	Package Style	TO-46/52, Dies, Custom Package
6	Lead Length	13.5 $\pm$ 0.5mm (TO-46/52)
7	Storage Temperature	-65°C to 135°C
8	Bare Die Size	2.0 mm x 2.5 mm x 0.675 mm
9	Response Time in still air using LCSR <sup>3</sup> method ( $\tau$ 63.2%)	40 sec (TO-46)
		3 sec (bare die, with lead wires)
10	Recommended values of excitation Current	0.1mA to 0.3mA
<p style="text-align: center;">R-T Calibration Polynomial<sup>4</sup></p> $R_T = R_0 (1 + AT + BT^2)$ <p style="text-align: center;"><math>R_T</math> = Resistance at Temperature T°C  <math>R_0</math> = Resistance at Temperature 0°C  A, B = Polynomial Coefficients</p>		

Note-1: Wider Temperature ranges are also available.

Note-2: Accuracy with calibration coefficients ( $R_0$ , A & B) in the range -20°C to 100 °C.

Note-3: LCSR (Loop Current Step Response). This response time corresponds to the package TO-46/52.

Note-4: Each sensor is individually calibrated with 0.1 mA of excitation current. Sensor comes with values of calibration coefficients  $R_0$ , A & B.

### Description

SCL's thin film temperature sensors are made of high purity platinum, which is deposited by E-beam evaporation system on silicon substrate. The sensing element was patterned using photolithographic process as per the design layout. The electrical connection between die pads to pin out through aluminum wire bonding using ultrasonic wire bonder.

PRT is a two terminal Pt- based resistance. Sensor resistance changes with temperature. Change in sensor resistance may be detected by known constant current excitation and reading back sensor voltage.

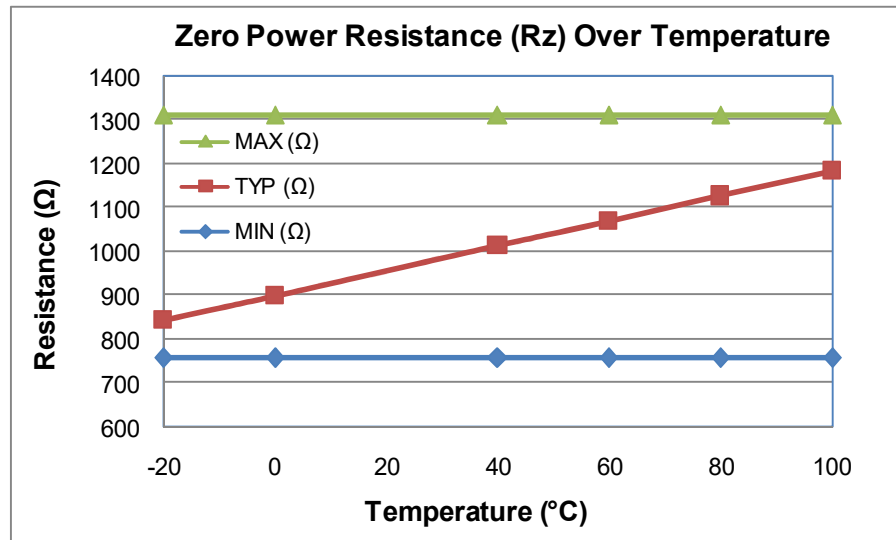
### Specifications

Platinum Resistance Temperature Sensor (PRT)	
Part No.	PRT-0900
Temperature Range	-20°C to 100 °C
Accuracy <sup>1</sup>	< 0.5°C
Nominal Resistance (at 0°C), R <sub>0</sub>	900 Ω
Nominal Temperature Coefficient, TCR	0.00315 Ω/Ω/°C
Package Style	TO-46/52 with Cap
Body Base Material	KOVAR Header with Nickel Cap
Lead Base Material	KOVAR
Weight (Maximum)	350 mg
Lead Length	13.5 ± 0.5mm
Storage Temperature	-65°C to 135°C
Response Time in still air using LCSR2 method (τ63.2%)	< 40 sec

Note-1: Worst case accuracy with calibration coefficients (R<sub>0</sub>, A & B) in the range -20°C to 100 °C.

Note-2: LCSR (Loop Current Step Response). This response time corresponds to the chosen package TO46.

### Zero Power Resistance & Temperature Characteristics



### Resistance vs. Temperature Calibration Polynomial

$$R_T = R_0 (1 + AT + BT^2)$$

$R_T$  = Resistance at Temperature  $T^{\circ}\text{C}$

$R_0$  = Resistance at Temperature  $0^{\circ}\text{C}$

A, B = Polynomial Coefficients

Each sensor is individually calibrated with 0.1 mA of measurement dc current.

### Absolute Maximum Ratings

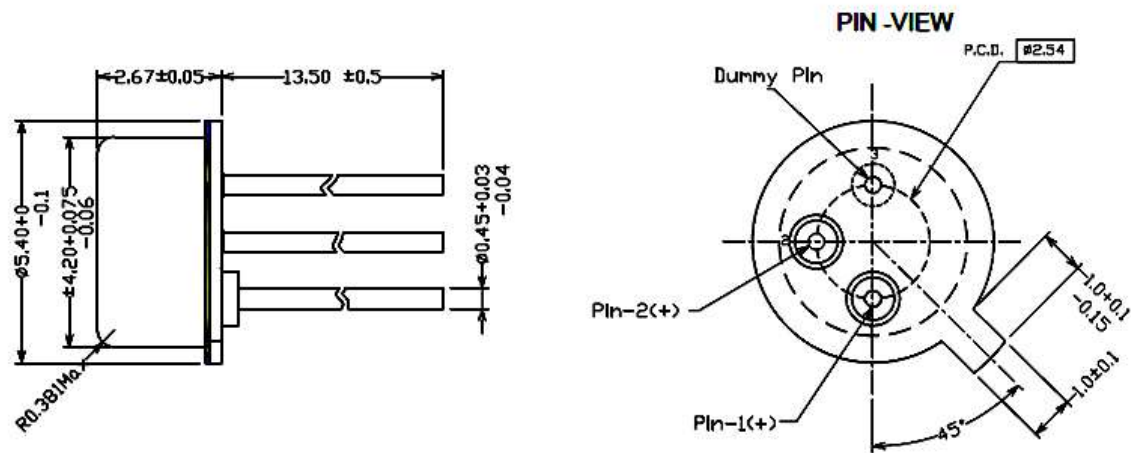
The maximum ratings shall not be exceeded at any time during use or storage

Parameter	Min.	Max.	Units
DC Measurement Voltage	-	0.76	Volts
DC Measurement Current	-	1.0	mA
Power dissipation (PD)		1.5	mW
Storage Temperature ( $T_{STG}$ )	-65	135	°C

#### Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating DC Current	-	0.1	0.3	mA
Zero Power Resistance ( $R_z$ ) at 0°C	810	900	990	$\Omega$
TC of Resistance (TCR)	0.00306	0.00315	0.00324	( $\Omega/\Omega/^\circ\text{C}$ )
Insulation Resistance	100	-	-	M $\Omega$
Operating Temperature ( $T_{AMB}$ )	-20	-	100	°C

Mechanical Drawing



All dimensions are in mm



## Annexure-C: Readout IC SC1218-0 Datasheet



# 4 DIFFERENTIAL CHANNELS, 24-BIT $\Sigma$ - $\Delta$ ANALOG-TO-DIGITAL CONVERTER (RADIATION HARDENED)

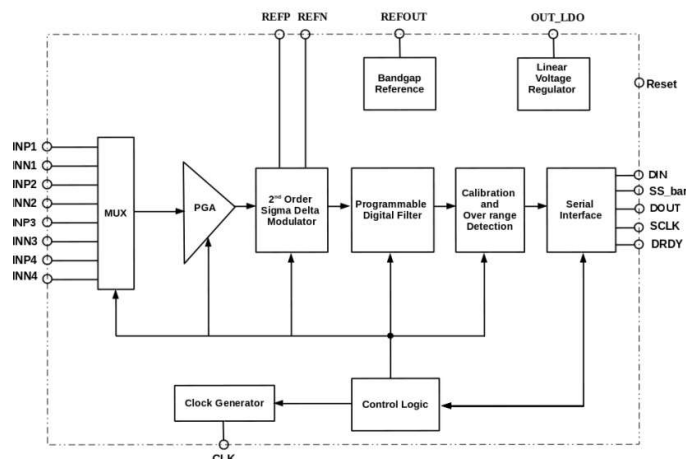
### FEATURES:

- 24 BITS NO MISSING CODES<sup>1</sup>
- 0.003% INL
- 19 BITS EFFECTIVE RESOLUTION (PGA = 1, OSR=2048)  
12 BITS (PGA = 128, OSR=2048)
- PGA FROM 1 TO 128 (BINARY STEPS)
- PROGRAMMABLE DATA OUTPUT RATES UP TO 19.5 KHz<sup>2</sup>
- PRECISION ON-CHIP 1.22V REFERENCE  
ACCURACY: 1.5%  
DRIFT:  $\pm 20$ ppm of REFOUT
- EXTERNAL DIFFERENTIAL REFERENCE Upto 2.5V
- ON-CHIP CALIBRATION
- SPI COMPATIBLE
- 3.0V TO 3.6V
- Rad Hardened (TID) upto 300 krad
- SEL/SEU immune upto 50 LET MeV-cm<sup>2</sup>/mg
- 180nm SCL CMOS standard logic process
- ESD Protection upto  $\pm 3$ KV HBM
- $\theta_{JC} = 3.7^{\circ}\text{C/W}$

### DESCRIPTION:

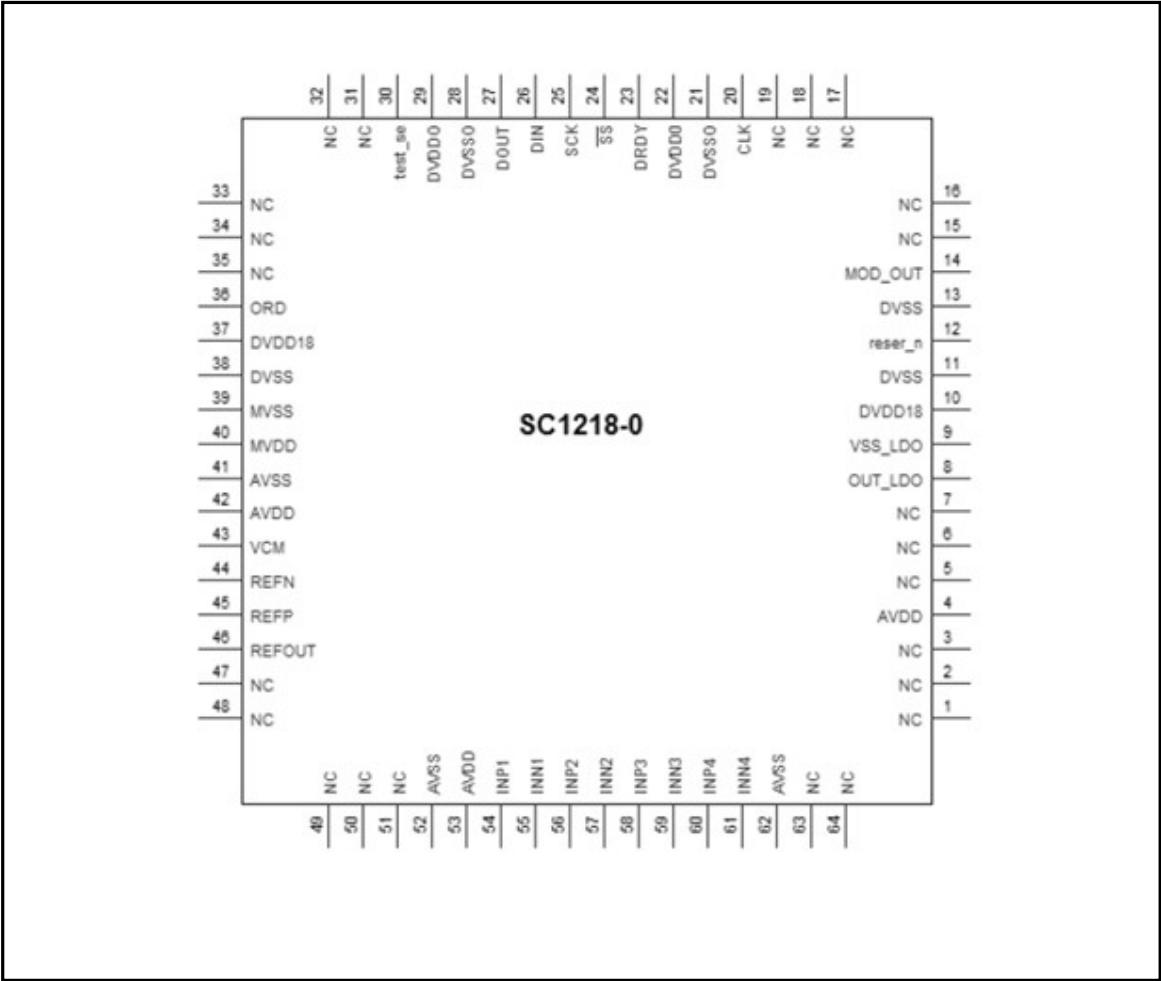
The SC1218-0 is a precision, wide range, Sigma-Delta, Analog-to-Digital converter with 24-bit resolution operating from 3.0V to 3.6V. It has fully four differential multiplexed channels. The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 in binary steps with an effective resolution of 19 bits at PGA 1 and OSR of 2048. It uses a second order Sigma Delta Modulator that converts the analog input signal in to a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output.

The decimation ratio of the digital filter can be programmed by user either to achieve higher accuracy or higher throughput. SC1218-0 has digitally on-chip offset and gain calibration. The serial interface is SPI Compatible. It can be configured to scan all the signal input sequentially with minimum communication overhead.



Notes: (1) Tested and verified upto 14 Bits.  
(2) 20MHz Clock Input

PIN CONFIGURATION:



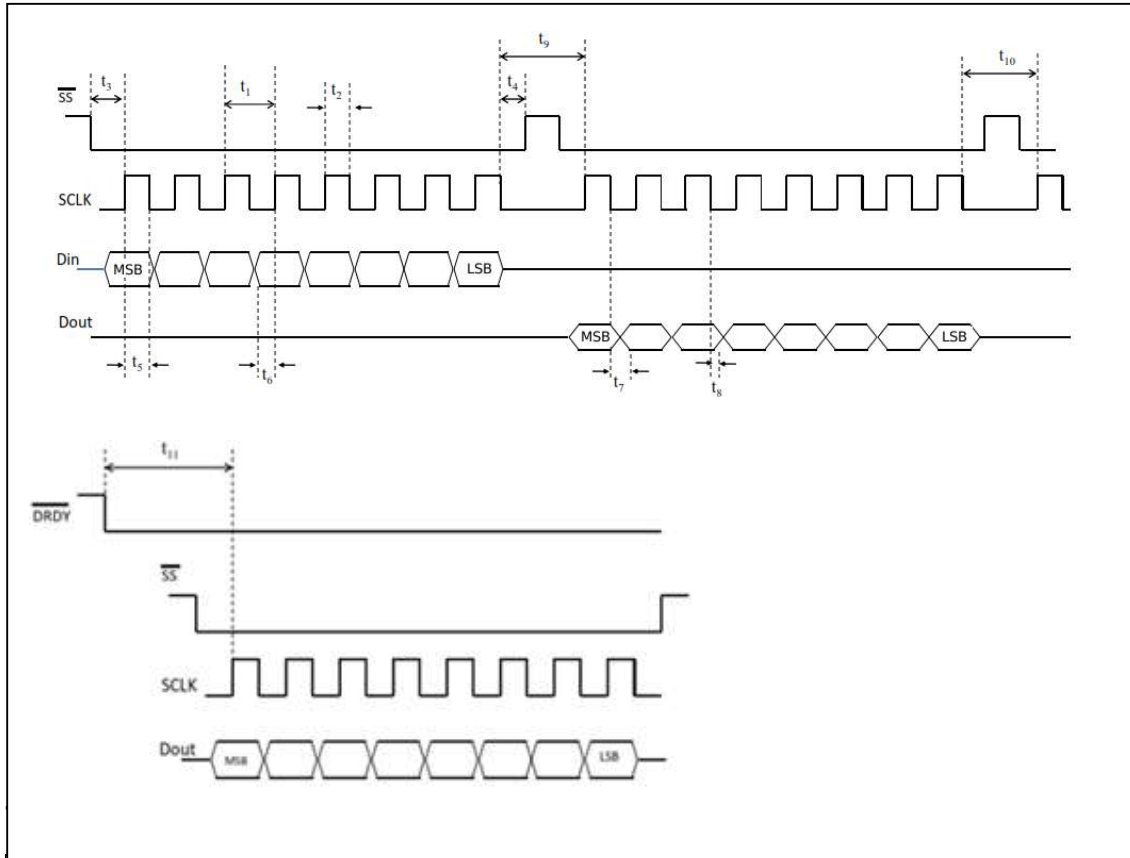
**PIN DESCRIPTIONS:**

PINNO.	NAME	DESCRIPTION
1	N.C.	Not Connected
2	N.C.	Not Connected.
3	N.C.	Not Connected
4	AVDD	Analog Core Power Supply(3.3V)
5	N.C.	Not Connected
6	N.C.	Not Connected.
7	N.C.	Not Connected
8	OUT_LDO	LDO Output (1.8V)
9	VSS_LDO	LDO Ground
10	DVDD18	Digital Core Power Supply(1.8V)
11	DVSS	Digital Core Ground
12	reset_n	Reset ,Active Low
13	DVSS	Digital Core Ground
14	MOD_OUT	Modulator Output (Test Pin). To be kept floating
15	N.C.	Not Connected
16	N.C.	Not Connected.
17	N.C.	Not Connected
18	N.C.	Not Connected.
19	N.C.	Not Connected
20	CLK	Clock Input
21	DVSSO	Digital I/O ground
22	DVDDO	Digital I/O Power Supply(3.3V)
23	DRDY	Data Ready, Active Low
24	SS	Serial Interface Enable, Active Low
25	SCLK	Serial Clock
26	DIN	Serial Data Input
27	DOUT	Serial Data Output
28	DVSSO	Digital I/O ground
29	DVDDO	Digital I/O Power Supply(3.3V)
30	test_se	Scan Enable
31	N.C.	Not Connected.
32	N.C.	Not Connected
33	N.C.	Not Connected
34	N.C.	Not Connected.
35	N.C.	Not Connected
36	ORD	Over Range Detection
37	DVDD18	Digital Core Power Supply(1.8V)
38	DVSS	Digital Core Ground
39	MVSS	Mixed Signal Ground
40	MVDD	Mixed Signal Power Supply(3.3V)
41	AVSS	Analog Core Ground
42	AVDD	Analog Core Power Supply(3.3V)
43	VCM	Common mode Voltage (1.65V) output Pin.
44	REFN	Negative Differential Reference Input
45	REFP	Positive Differential Reference Input
46	REF_OUT	Output of Band Gap Reference
47	N.C.	Not Connected.
48	N.C.	Not Connected
49	N.C.	Not Connected
50	N.C.	Not Connected.
51	N.C.	Not Connected
52	AVSS	Analog Core Ground



<b>53</b>	AVDD	Analog Core Power Supply(3.3V)
<b>54</b>	INP1	Multiplexer Positive Input of channel1.
<b>55</b>	INN1	Multiplexer Negative Input of channel1.
<b>56</b>	INP2	Multiplexer Positive Input of channel2.
<b>57</b>	INN2	Multiplexer Negative Input of channel2.
<b>58</b>	INP3	Multiplexer Positive Input of channel3.
<b>59</b>	INN3	Multiplexer Negative Input of channel3.
<b>60</b>	INP4	Multiplexer Positive Input of channel4.
<b>61</b>	INN4	Multiplexer Negative Input of channel4.
<b>62</b>	AVSS	Analog Core Ground
<b>63</b>	N.C.	Not Connected.
<b>64</b>	N.C.	Not Connected

## TIMING SPECIFICATIONS:



SPEC	DESCRIPTION	MIN	MAX	UNIT
$t_1$	SCLK period	4 cycle		$t_{CLK}$ Period
$t_2$	SCLK pulse width (High and Low)	2 cycle		$t_{CLK}$ Period
$t_3$	$\overline{SS}$ low to first SCLK edge	100		ns
$t_4$	Last SCLK falling edge to $\overline{SS}$ HIGH	100		ns
$t_5$	SCLK rising edge to DIN valid (Hold time)	50		ns
$t_6$	DIN valid to SCLK rising edge (Setup time)	50		ns
$t_7$	SCLK falling Edge to valid new Dout		50	ns
$t_8$	SCLK falling Edge to DOUT, Hold Time	0		ns <sup>z</sup>
$t_9$	Delay between last SCLK edge of 1st byte transfer and first SCLK edge for subsequent 2nd byte transfer : RDATA, RDATA, RREG, WREG Command	50		$t_{CLK}$ Period
$t_{10}$	Final SCLK edge of one command until first edge SCLK of next command	4		$t_{CLK}$ Period
$t_{11}$	DRDY LOW to first SCLK edge of first byte transfer for RDATA command	15		$t_{CLK}$ Period
$t_{11}$	DRDY LOW to first SCLK edge of first byte transfer for RDATA command	0		$t_{CLK}$ Period

Notes: (1) DOUT goes immediately into tri-state whenever  $\overline{SS}$  is high (2) DOUT should be sampled externally on rising edge of SCLK. DOUT will remain valid till next falling edge.

## ELECTRICAL CHARACTERISTICS

All Specifications AVDD, MVDD, DVDDO= +3.3V, DVDD18 = +1.8V, Temp. = 25°C, OSR=2048,  $f_{MOD}$  = 78.125 KHz,  $f_{CLK}$  = 2.5MHz, PGA=1,  $f_{Data}$  = 38.147Hz, REF IN+ =2.65V, REF IN- =0.65V, unless otherwise specified.

PARAMETER	TESTS CONDITIONS	SC1218-0			UNITS
		MIN	TYP	MAX	
<b>ANALOG</b>					
Analog Input Range	$V_{INP}-V_{INN}$ User Selectable	0		AVDD	V
Full Scale Input Range		$-V_{REF}/PGA$		$+V_{REF}/PGA$	V
Programmable Gain Amplifier		1		128	
Static Input Current			2	1.0	μA
Input Capacitance					pF
Bandwidth					
Sinc <sup>3</sup> Filter***	-3dB		$0.262 * f_{Data}$		Hz
Differential Input Impedance	Modulator Frequency=78KHz		100		KΩ
<b>DEVICE PERFORMANCE</b>					
Resolution	OSR=512, $f_{CLK}$ =5MHz, $f_{MOD} = f_{CLK} /32$ Best Fit Method	24			Bits
No Missing Code*		14		±0.003	Bits % of FS
Integral Non-Linearity					
Offset Error**	Before Calibration			220	ppm of FS
Offset Drift	-40°C to +125°C			0.22	ppm of FS/°C
Gain Error	Before Calibration			0.225	% of FS
Gain Drift	-40°C to +125°C			0.303	ppm /°C
Effective Number of Bits (ENOB)	Based on 100 samples			19	Bits
Common-Mode Rejection	At DC		102		dB
	$f_{CM}=10Hz, f_{DATA}=30Hz$		89		dB
	$f_{CM}=100Hz, f_{DATA}=30Hz$		89		dB
	$f_{CM}=1KHz, f_{DATA}=30Hz$		95		dB
Power Supply Rejection	DC, dB = $-20 \log(\Delta V_{OUT} / \Delta V_{DD})$		77		dB
	$V_{ac}=\pm 660mV_{P-P}, 10Hz, f_{DATA}=30Hz$		58		dB
	$V_{ac}=\pm 660mV_{P-P}, 100Hz, f_{DATA}=30Hz$		59		dB
	$V_{ac}=\pm 660mV_{P-P}, 1KHz, f_{DATA}=30Hz$		60		dB
<b>ON CHIP VOLTAGE REFERENCE</b>					
Output Voltage	No Load	1.2	1.22	1.24	V
Drift				±20	ppm/°C
Start up Time***				50	μS
Load Regulation	@Full Load Current = 2.5mA			1.0	%
<b>VOLTAGE REFERENCE INPUT</b>					
VREF	(REFIN+)-(REFIN-)		2.0	2.5	V
<b>CLOCK INPUT****</b> $f_{CLK}$			2.5	20	MHz
<b>POWER SUPPLY REQUIREMENT</b>					
Supply Voltage	AVDD, DVDDO, MVDD DVDD18	3.0 1.62	3.3 1.8	3.6 1.98	V V
Analog Current			6.2	7	mA
Digital Current			1000	1500	μA
<b>ON CHIP LDO</b>					
Output Voltage	OUT_LDO	1.755	1.80	1.845	V
No Load Current			4.5		mA
Line Regulation				0.5	%
Load Regulation	@Full Load Current = 11mA			0.05	%
Temp Drift	-55°C to +125°C			±100	ppm/°C
<b>TEMPERATURE RANGE</b>					
Operating		-55		125	°C
<b>Total Ionize Dose</b>	Upto 300KRad		Pass		
<b>Single Event Effect</b>					
Single Event Latch up	Upto 50 LET (MeV-cm <sup>2</sup> /mg)		Pass		
Single Event Upset	Upto 50 LET (MeV-cm <sup>2</sup> /mg)		Pass		

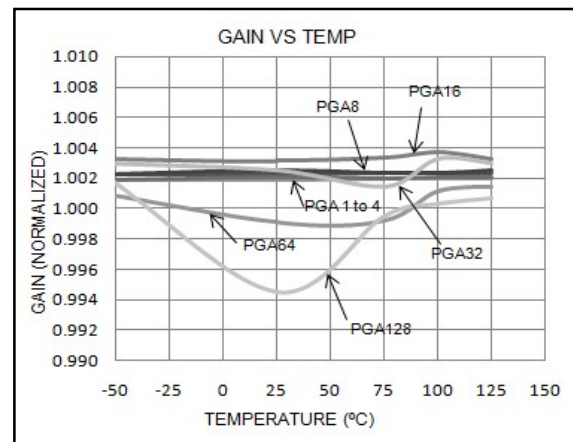
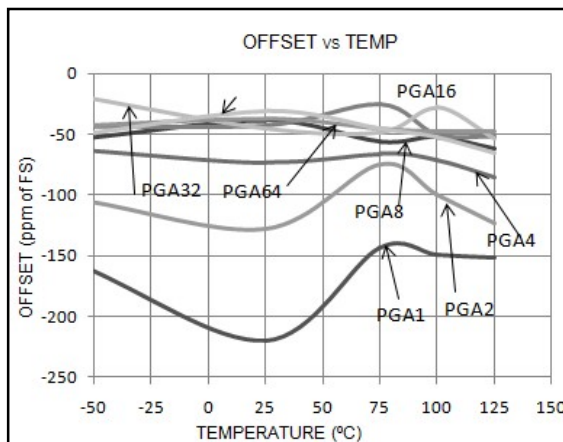
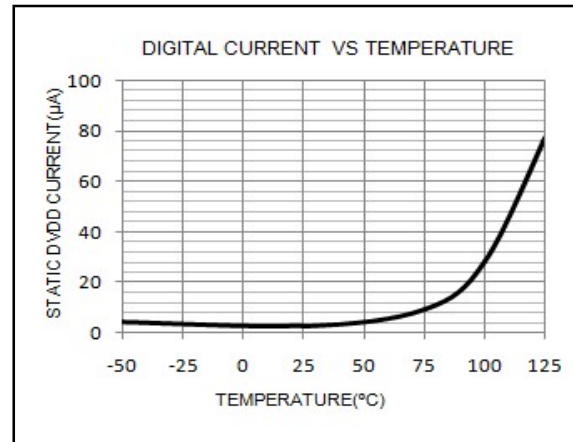
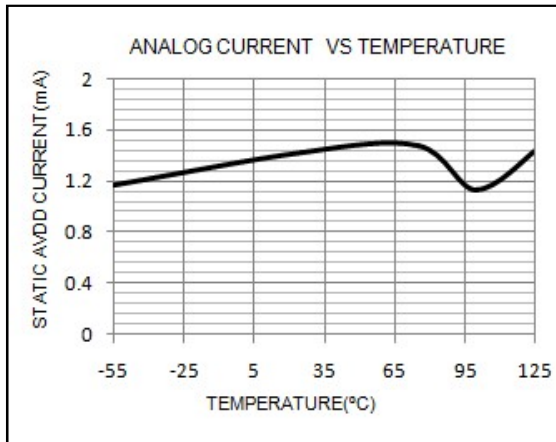
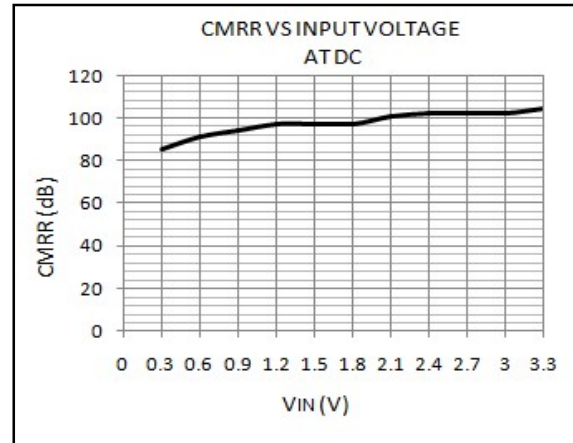
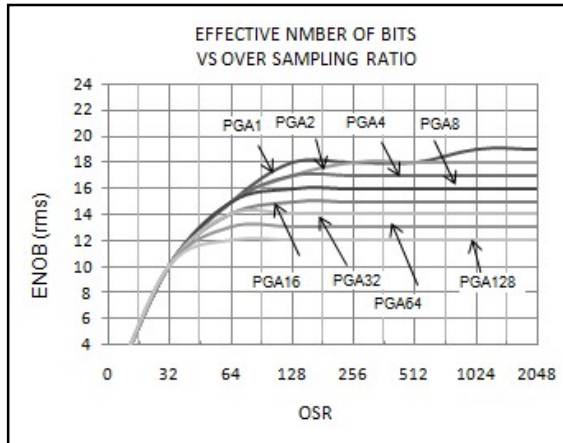
\*Missing codes are verified and tested upto 14bits. Device may perform for better results.

\*\*Calibration can minimize this error.

\*\*\*Simulated Result

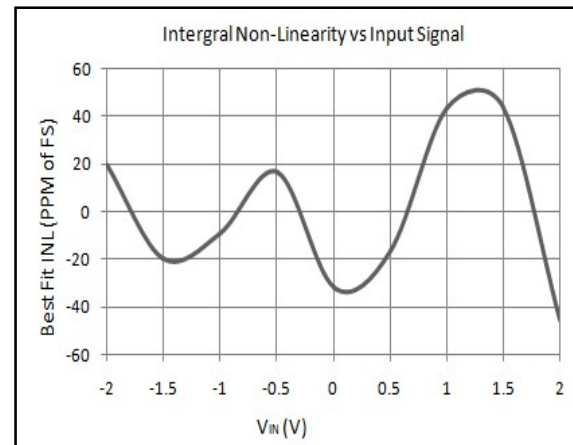
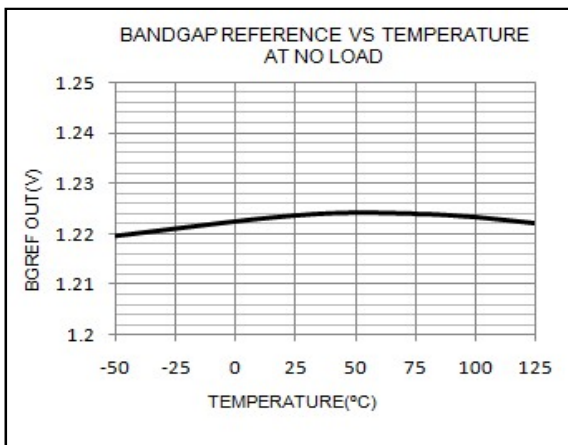
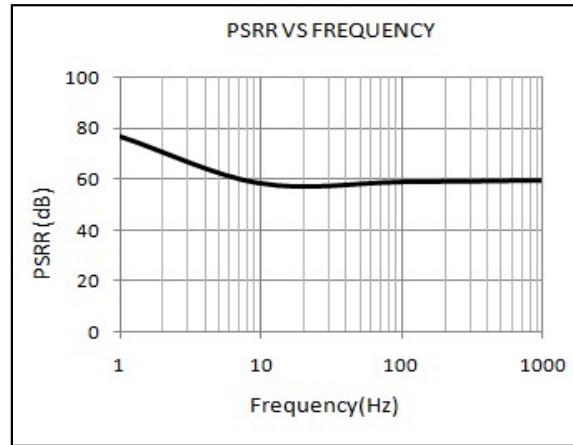
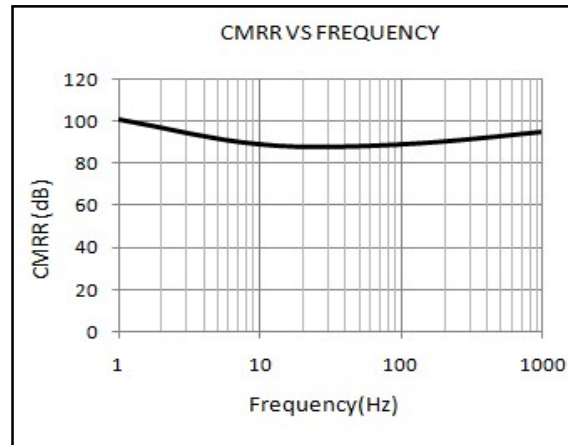
## ELECTRICAL CHARACTERISTICS

All Specifications AVDD, MVDD, DVDD0 = +3.3V, DVDD18 = +1.8V, Temp. = 25°C, OSR=2048,  $f_{MOD}$  = 78.125 KHz,  $f_{CLK}$  = 2.5MHz, PGA=1,  $f_{Data}$  = 38.147Hz, REF IN+ = 2.65V, REF IN- = 0.65V, unless otherwise specified.



## ELECTRICAL CHARACTERISTICS

All Specifications AVDD, MVDD, DVDDO= +3.3V, DVDD18 = +1.8V, Temp. = 25°C, OSR=2048,  $f_{MOD} = 78.125$  KHz,  $f_{CLK} = 2.5$  MHz, PGA=1,  $f_{Data} = 38.147$  Hz, REF IN+ =2.65V, REF IN- =0.65V, unless otherwise specified.



## DIGITAL CHARACTERISTICS

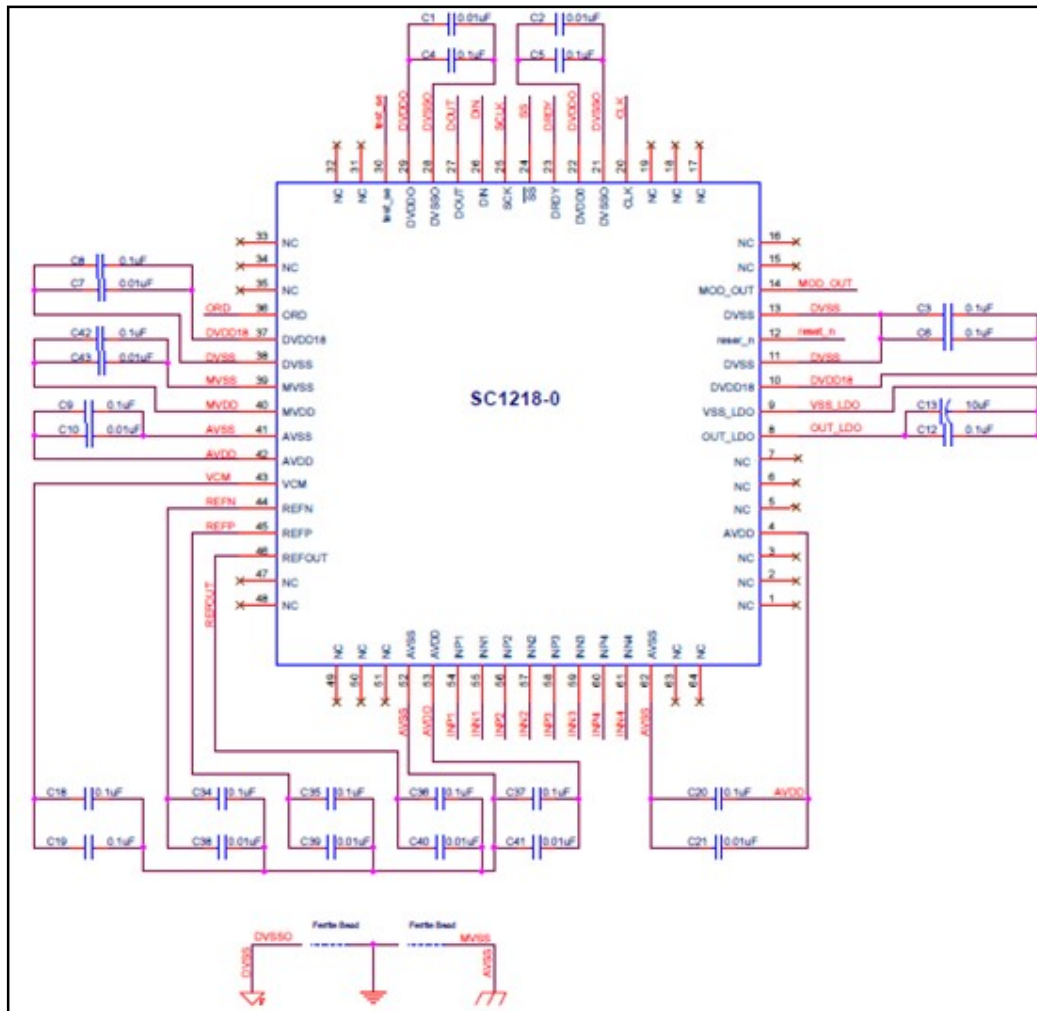
DVDDO= 3.0V to 36V

PARAMETER	TESTS CONDITIONS	SC1218-0			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: $V_{IH}$		2		DVDDO	V
$V_{IL}$		DVSS		0.8	V
$V_{OH}$	$I_{OH}=8mA$	3.0			V
$V_{OL}$	$I_{OL}=8mA$	DVSS		0.4	V
Input Leakage: $I_{IH}$	$V_I=DVDDO$			1	$\mu A$
$I_{IL}$	$V_I=DVSS$	-1			$\mu A$

## ABSOLUTE MAXIMUM RATING

PARAMETER	SC1218-0		UNITS
	MIN	MAX	
AVDD to AVSS	-0.3	4.3	V
DVDDO to DVSS	-0.3	4.3	V
DVDD18 to DVSS	-0.3	2.2	V
INP, INN	-0.3	AVDD+0.3	V
Digital Input Voltage to DGND	-0.3	DVDDO+0.3	V
Digital Output Voltage to DVSS	-0.3	DVDDO+0.3	V
Digital Output Current		8	mA
Maximum Ambient Temperature		125	°C

## TEST CIRCUIT DIAGRAM



## PCB LAYOUT RECOMMENDATION

The test / application board should be four layer PCB. To achieve highest level of performance, surface-mount components to be used wherever possible. This reduces the trace length and minimizes the effects of parasitic capacitance and inductance. The board should use separate ground with all the analog signals and the digital signals. Bypass capacitors are strongly recommended at power supply and reference pins of the converter. User should also use R-C filter (49.9Ω and 47pF) on each input to have better performance.

## OVERVIEW

### INPUT MULTIPLEXER

The input analog multiplexer can select any of the four differential inputs. The output of the multiplexer is connected internally to ADC input. Analog multiplexer channel can be selected by setting MSEL1:MSEL0 bits in CR1 control register.

### PROGRAMMABLE GAIN AMPLIFIER

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64 or 128. Adjusting the internal gain of a sigma delta modulator is a technique, which can be used to get an appropriate LSB size for the transducers application. It will improve the resolution of the ADC. PGA gain can be selected by setting PGA2:PGA0 bits in CR1 control register.

### MODULATOR

A second order single loop sigma delta modulator is used in the Sigma Delta ADC. The sigma delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The integrators used in the modulator are switched capacitor based. The first integrator of the modulator is auto-zeroed.

The modulator runs at clock frequency  $f_{MOD}$  that can be adjusted by setting the appropriate value of PRE1: PRE0 of CR2 control register as shown in the following table:

PRE1:PRE0	$f_{MOD}$
00	$f_{CLK} / 16$
01	$f_{CLK} / 32$
10	$f_{CLK} / 64$
11	$f_{CLK} / 128$

Where  $f_{CLK}$  is external clock frequency

The modulator is designed to work at a maximum sampling frequency of 625 KHz. The output of modulator is available at MOD\_OUT pin for the diagnosis purpose.

### PROGRAMMABLE DIGITAL FILTER

The on-chip digital filter processes the single bit data stream from the modulator using a sinc3 filter. The sinc filters are conceptually simple, efficient and flexible, especially where variable resolution and data rates are required. Output data rate of digital filter can be programmed by setting OSR2:OSR0 bits of CR2 control register.

OSR2:OSR0	Output Data Rate
000	$f_{MOD} / 2048$
001	$f_{MOD} / 1024$
010	$f_{MOD} / 512$
011	$f_{MOD} / 256$
100	$f_{MOD} / 128$
101	$f_{MOD} / 64$
110	$f_{MOD} / 32$

Whenever there is step change in input or MUX selection, digital filter requires three cycles to settle.

### DRDY (DATA READY)

The DRDY pin is used as a status signal to indicate when new digital code is ready to read. DRDY goes low when new data is available. It becomes high when a read operation from the data register is executed using RDATA or RDATA\_C command. The DRDY pin goes high at the middle of read of 2<sup>nd</sup> MSB byte. In case, when no read operation is performed, DRDY will remain low.

### BANDGAP REFERENCE

The device has on chip 1.2V bandgap reference circuitry. To use it, the user needs to connect it externally with ADC reference pins.

## SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (DIN, DOUT, SCLK and SS). SCLK frequency can go up to  $f_{CLK}/4$ . If SS pin goes HIGH the serial interface will reset and DOUT pin will become tri-state.

The SS must be LOW during the communication. DIN is the serial data input port. It is internally sampled at positive edge of SCLK by SPI. DOUT is the serial data output port and is launched at negative edge of SCLK.

SS pin can be tied low to use SPI as 3-wire interface.

## OFFSET AND GAIN CALIBRATION

Both self offset error in SC1218-0 device or complete system offset error can be reduced with offset calibration. This is handled with two offset commands SEFOCAL and SYSOCAL. There is also a gain calibration module to compensate system gain error with commands SELFGAIN and SYSGAIN. **Please refer calibration procedure section.** Each calibration process takes five conversion cycles to complete. Calibration must be performed after system reset, a change in decimation ratio or a change of the PGA.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to apply gain correction, GCALEN bit has to be set. SELFGAIN command is only applicable at PGA1.

## OVER-LOAD DETECTION MODULE

Where digital code without calibration is such that it cannot be corrected after calibration then Over-Load detection module detects over-load and clip digital output appropriately to 7FFFFFF<sub>H</sub> and 800000<sub>H</sub>.

Status of over-load detection module is available at ORD Pin. This pin will become high in case of over-load condition.

Over-load detection can be disabled by setting OLDD flag of CR2 control register. By default it is enabled.

## OVER-RANGE DETECTION MODULE

If digital code after gain and offset calibration is out of the acceptable code range then digital over-range module detects over-range and clip digital output appropriately to 7FFFFFF<sub>H</sub> and 800000<sub>H</sub>. To ensure the proper functioning of the Over Range Detection Module, following constraint on OCR & FSR register value must be followed:

Maximum value of OCR register should not exceed 3FFFFFF<sub>H</sub> for negative offset correction and C00000<sub>H</sub> for positive offset correction. FSR value must be positive.

When device is in the over-range condition, the ORD pin will become high.

Over-range detection can be disabled by setting OVDD flag of CR2 control register. By default it is enabled.

OVDD bit also affects digital output range. Setting OVDD bit will half the digital output range as shown below.

OVDD BIT	ANALOG INPUT	DIGITAL OUTPUT CODE
0	+V <sub>REF</sub>	7FFFFFF <sub>H</sub>
	0	000000 <sub>H</sub>
	-V <sub>REF</sub>	800000 <sub>H</sub>
1	+V <sub>REF</sub>	3FFFFFF <sub>H</sub>
	0	000000 <sub>H</sub>
	-V <sub>REF</sub>	C00000 <sub>H</sub>



## CALIBRATION PROCEDURE

The SC1218-0 device has two commands namely SEFOCAL and SYSTEMOCAL to compensate offset errors. Internal calibration of device is called self calibration. By executing SELFOCAL command, the device shorts the ADC input and stores the offset value into OCR register in 2's complement form.

For system calibration, the user must apply appropriate 'zero signal' to the selected input channel and then execute SYSOCAL command. In this case ADC computes the offset value based on the available differential input signal and stores it into OCR register in 2's complement form. The System gain calibration requires appropriate "full scale differential input signal. On executing system gain command, ADC computes a value to nullify gain error.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to enable gain calibration set GCALEN bit of CR1 register. Each calibration process

takes five conversion cycles to complete. DRDY will be asserted to indicate completion of the calibration process.

Apart from above commands, OSR and FSR can be accessed externally through RREG (Read Register) and WREG (Write Register) commands. This will provide flexibility to manually set the OCR and FSR.

When FSR is externally loaded, follow the procedure as below.

- Perform Self/System gain calibration as stated above and read the FSR register and note down the value.
- Divide FFFFFFFC00000 by noted value of FSR register and take its integer portion.
- This calculated value has to be written into FSR register at next power ON in order to perform gain calibration without command.

For example:

Let noted value of FSR register is 3ee259.

The value to be written in the FSR reg. after power off and on will be:

$$\text{FFFFFFC00000}/3\text{ee}259 = 4122\text{B7}.$$

## COMMAND DEFINITIONS

The commands listed below control the operation of SC1218-0 Device. Some commands are stand-alone commands (e.g. STOPC) while others require additional bytes(e.g., WREG requires command and the data bytes).

Operands:

rrrr represents the register address.

nnnnnnnn represents the data.

xxxx: these bits will be ignored while instruction decoding.

COMMANDS	DESCRIPTION	COMMANDBYTE	2 <sup>ND</sup> COMMANDBYTE
RDATA	Read Data	0001 xxxx (1x <sub>H</sub> )	-N.A.-
RDATA C	Read Data Continuously	0010 xxxx (2x <sub>H</sub> )	-N.A.-
STOPC	Stop Read Data Continuously	0011 xxxx (3x <sub>H</sub> )	-N.A.-
RREG	Read from Register rrrr	0100rrrr(4r <sub>H</sub> )	-N.A.-
WREG	Write to Register rrrr	0101rrrr(5r <sub>H</sub> )	nnnnnnnn
SELFOCAL	Self Offset Calibration	0110xxxx(6x <sub>H</sub> )	-N.A.-
SYSOCAL	System Offset Calibration	0111xxxx(7x <sub>H</sub> )	-N.A.-
SELF GAIN	Self Gain Calibration	1000xxxx(8x <sub>H</sub> )	-N.A.-
SYS GAIN	System Gain Calibration	1001xxxx(9x <sub>H</sub> )	-N.A.-

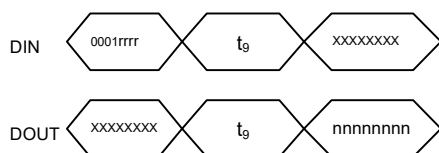
### RREG (READREGISTER)

RREG (Read Register) command reads content of the specified register. The address of the register to be read is specified in the LSB nibble of the instruction.

Operands: r, n

Bytes: 2

Encoding: 0100 rrrr



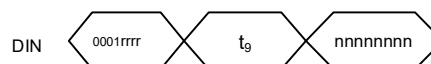
### WREG (WRITE REGISTER)

WREG (Write Register) command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the first byte. Second byte represents the data to be written.

Operands: r, n

Bytes: 2

Encoding: 0101rrrr nnnnnnnn



### RDATA (READDATA)

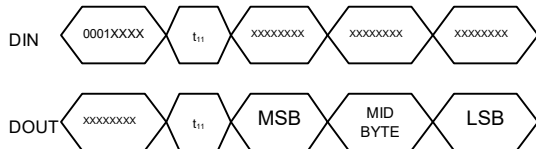
This command reads a single 24-bit ADC conversion result. In response to RDATA command ADC transmit 24-bit digital code. Digital code is available at DOUT pin in 8-bit format with most significant byte first. RDATA command must be followed by 3-byte read

operation. On completion of read operation, DRDY goes high.

Operand: x

Bytes: 1

Encoding: 0001 xxxx



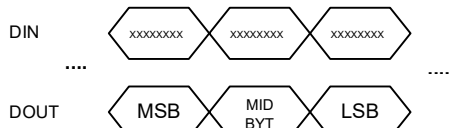
### RDATAC (READ DATA CONTINUOUS)

RDATAC command enables the continuous output of new data on each DRDY. This command eliminates the need to send the Read Data Command on each DRDY. In case of read data continuous command user can directly perform 3 read operation to read 24-bit digital code. DRDY will go high in response to 3-byte read operation. RDATAC command must be followed by STOPC command before issuing any other command.

Operand: x

Bytes: 1

Encoding: 0010 xxxx



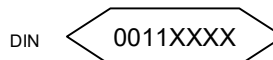
### STOPC (STOP READ DATA CONTINUOUS)

This command ends the continuous data output mode. After this command DRDY will also go high.

Operands: x

Bytes: 1

Encoding: 0011 xxxx



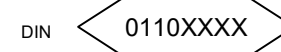
### SELFOCAL (SELF OFFSET CALIBRATION)

This command performs Self Offset Calibration. At the end of the calibration process, offset value will be stored in 24-bit internal Offset Calibration Register (OCR) in 2's complement format. DRDY will be asserted low to indicate completion of the command.

Operands: x

Bytes: 1

Encoding: 0110 xxxx



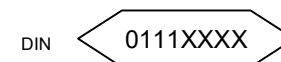
### SYSOCAL (SYSTEM OFFSET CALIBRATION)

With this command ADC computes the offset value based on the available differential input signal on selected analog channel to nullify offset in the system. The offset value will be stored in 24-bit internal Offset Calibration Register (OCR) in 2's complement format. DRDY will be asserted low to indicate completion of the command.

Operands: x

Bytes: 1

Encoding: 0111xxxx



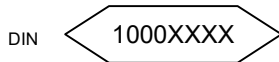
### **SELF GAIN (SELF GAIN CALIBRATION)**

This command performs Self Gain Calibration. At the end of the calibration process, gain calibration coefficient value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x

Bytes: 1

Encoding: 1000 xxxx



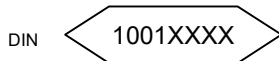
### **SYSGAIN (SYSTEM GAIN CALIBRATION)**

With this command ADC computes the gain value based on the available differential input signal on selected analog channel to nullify gain error in the system. The gain value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x

Bytes: 1

Encoding: 1001xxxx



## CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

Address	Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0 <sub>H</sub>	DIGITAL_CODE_B3(R)	DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16
1 <sub>H</sub>	DIGITAL_CODE_B2(R)	DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8
2 <sub>H</sub>	DIGITAL_CODE_B1(R)	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
3 <sub>H</sub>	CR1 (RW)	PGA2	PGA1	PGA0	OCEN	GCALEN	-	MSEL1	MSEL0
4 <sub>H</sub>	CR2(RW)	ACSEN	OLDD	OVDD	PRE1	PRE0	OSR2	OSR1	OSR0
8 <sub>H</sub>	OCR1(RW)	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
9 <sub>H</sub>	OCR2(RW)	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
A <sub>H</sub>	OCR3(RW)	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
B <sub>H</sub>	FSR1(RW)	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
C <sub>H</sub>	FSR2(RW)	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
D <sub>H</sub>	FSR3(RW)	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

R: Read only registers RW: Read/Write registers

Note: At reset all registers are initialized to 00<sub>H</sub>.

### CR1 (ADD: 03<sub>H</sub>) CONTROLREGISTER-1

BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0

PGA2	PGA1	PGA0	OCEN	GCALEN	-	MSEL1	MSEL0
------	------	------	------	--------	---	-------	-------

BIT 7-5: PGA2:PGA1:PGA0: Programmable Gain Amplifier selection

000=1      100 = 16  
 001=2      101 = 32  
 010= 4      110 = 64  
 011= 8      111 = 128

Bit4: OCEN: Offset Calibration Enable bit

OCE = 1: Enable offset calibration  
 OCE = 0: Disable offset calibration

Bit3: GCALEN: Gain calibration Enable bit

GCALEN = 1: Enable Gain calibration  
 GCALEN = 0: Disable Gain calibration

Bit1-0: MSEL1: MSEL0: Analog Channel Selection

00 = Channel-0      10 = Channel-2  
 01 = Channel-1      11 = Channel-3

**Note:** Any update in CR1 or CR2 control register will reset modulator and digital filter. DRDY will also go high.

### CR2 (ADD: 04<sub>H</sub>) CONTROL REGISTER- 2

BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0

-	OLDD	OVDD	PRE1	PRE0	OSR2	OSR1	OSR0
---	------	------	------	------	------	------	------

Bit6: OLDD: Analog over range detection

0 = Enable over-load detection.  
 1 = Disable over-load detection.

Bit5: OVDD: Digital over range detection

0 = Enable over-range detection.  
 1 = Disable over-range detection.

Bit4-2: PRE2:PRE1:PRE0: Prescaler bits

PRE1:PRE0	$f_{MOD}$
00	$f_{CLK} / 16$
01	$f_{CLK} / 32$
10	$f_{CLK} / 64$
11	$f_{CLK} / 128$

Bit2-0:OSR2:OSR0: OSR control bits.

000 = 2048 OSR  
 001 = 1024 OSR  
 010 = 512 OSR  
 011 = 256 OSR  
 100 = 128 OSR  
 101 = 64 OSR  
 110 = 32 OSR

**OCR1 (ADD: 08<sub>H</sub>) OFFSET CALIBRATION  
REGISTER-1 (Least Significant Byte)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

**OCR2 (ADD: 09<sub>H</sub>) OFFSET CALIBRATION  
REGISTER-2 (Middle Byte)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

**OCR3 (ADD: 0A<sub>H</sub>) OFFSET CALIBRATION  
REGISTER-3 (Most Significant Byte)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

**FSR1 (ADD: 0B<sub>H</sub>) FULL SCALE  
REGISTER-1 (Least Significant Byte)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

**FSR2 (ADD: 0C<sub>H</sub>) FULL SCAEE REGISTER-2  
(Middle Byte)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

**FSR3 (ADD: 0D<sub>H</sub>) FULL SCAEE REGISTER-3  
(Most Significant Byte)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

**DIGITAL\_CODE\_B3 (ADD: 00<sub>H</sub>) DIGITAL  
OUTPUT CODE  
(MOST SIGNIFICANT BYTE)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

**DIGITAL\_CODE\_B2 (ADD: 01<sub>H</sub>) DIGITAL  
OUTPUT CODE  
(MIDDLE BYTE)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08

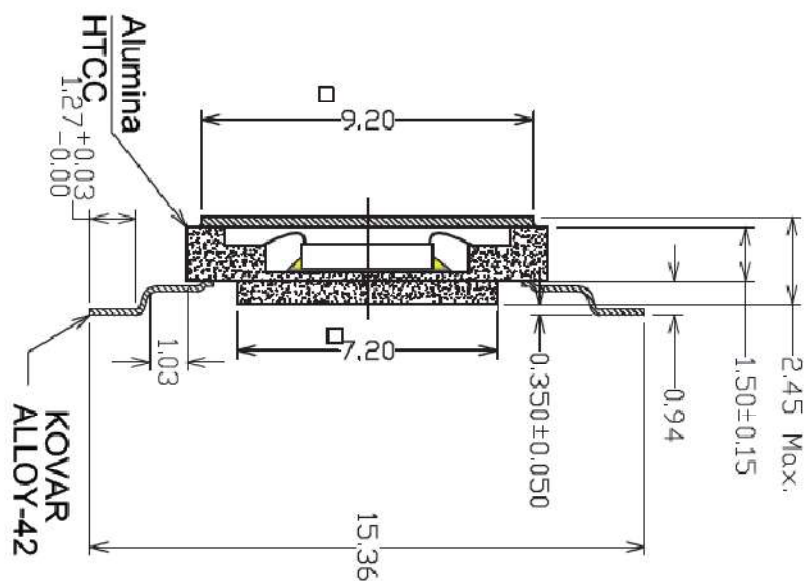
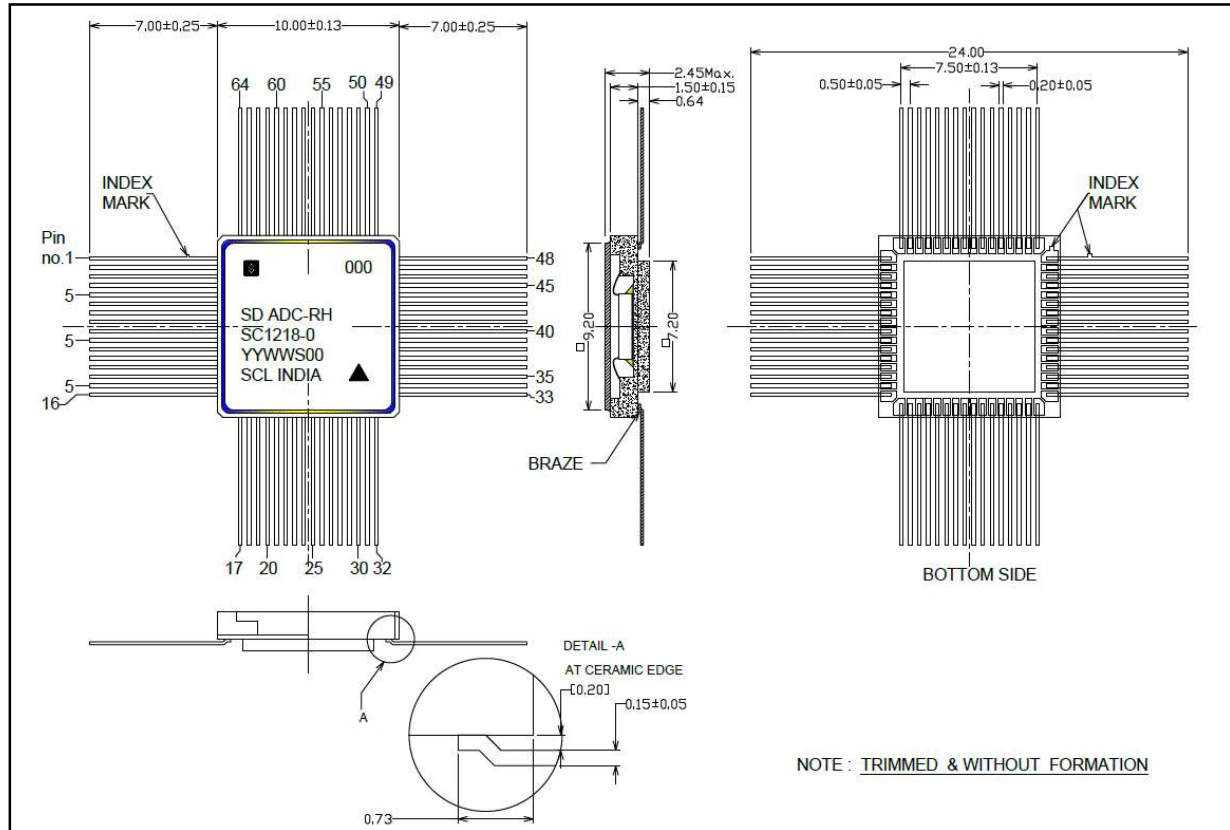
**DIGITAL\_CODE\_B1 (ADD: 02<sub>H</sub>) DIGITAL  
OUTPUT CODE  
(LEAST SIGNIFICANT BYTE)**

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00



## PACKAGE INFORMATION

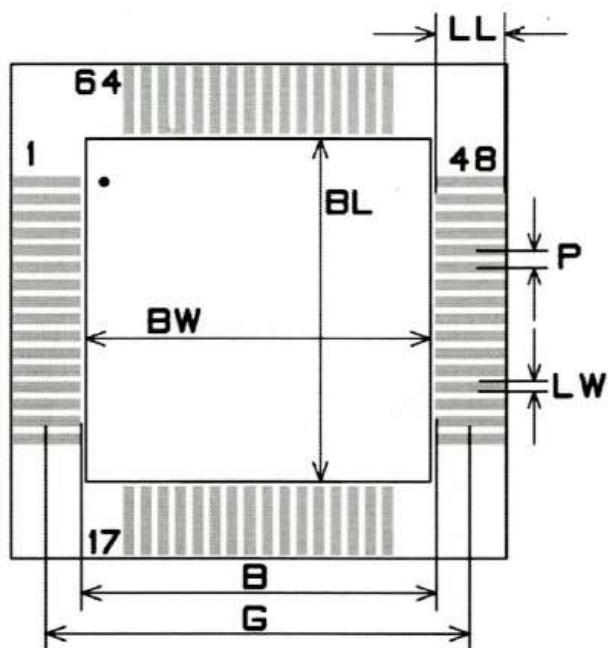
### CERAMIC QUAD FLAT PACKAGE (CQFP-64)



Note:



## PCB FOOTPRINT (LAND PATTERN)



Device Drawing Title	Device Drawing Number	P	LL	LW	G	B	Part No.	Height (max.)
Sigma Delta ADC RH SC1218-0 (64 PIN CQFP)	A1542050170	0.50	2.60	0.30	13.4	10.80	SC1218-0	2.45

### Note:

1. All Dimensions are in mm
2. Device body material is ceramic
3. Device body size BL X BW is 10.13 mm x 10.13 mm (maximum)





## TERMS AND DEFINITIONS

### Common-Mode Rejection Ratio (CMRR)

Common-mode rejection is the ability of a device to reject a signal that is common to both inputs. The Common mode signal can be an AC or DC signal, or a combination of the two. Common-mode rejection ratio (CMRR) is the ratio of the differential signal gain to the common-mode signal gain.

### Oversampling

For an ADC, sampling the analog input at a rate much higher than the Nyquist frequency is called oversampling. Oversampling improves the ADC's dynamic performance by effectively reducing its noise floor. Improved dynamic performance leads, in turn, to higher resolution. Oversampling is the basis of sigma-delta ADCs.

### Power-Supply Rejection (PSR)

Power Supply Rejection Ratio (PSRR) is the ratio of the change in DC power supply voltage to the resulting change in full-scale error, expressed in dB.

### Resolution

ADC resolution is the number of bits used to represent the analog input signal.

### Differential Nonlinearity (DNL) Error

For an ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB is defined as DNL.

### Gain Error

The gain error of an ADC or DAC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale range (%FSR), and it can be calibrated out with hardware or in software. Gain error is the full-scale error minus the offset error.

### Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature.

### Integral Nonlinearity (INL) Error

For data converters, INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the endpoints of the transfer function. INL is often called 'relative accuracy.'

### No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.



## TEST METHODS

**On chip reference test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Wait for 1 to 5ms. Sink zero current (or  $<1\mu\text{A}$ ) from REFOUT pin and measure REFOUT voltage (No load Output). Fail if measured voltage is not within given limits. Similarly sink 2.5mA current from REFOUT in and measure REFOUT voltage (Full Load Output). Fail if it is not within limits. Calculate load regulation as given below

$$\text{Load Regulation} = \frac{\text{No load output} - \text{full load output}}{\text{No load Output}} * 100$$

Check the load regulation value for pass/fail limit.

**On chip LDO test:** Apply AVDD, DVDDO, MVDD and VDD\_LDO equal to 3.3V. Apply DVDD18 equal to 1.8V. Wait for 1 to 5ms. Sink zero current (or  $<1\mu\text{A}$ ) from OUT\_LDO pin. Measure VDD\_LDO current and OUT\_LDO voltage. Fail if measured values are not within given limits. Similarly sink 11 mA current from OUT\_LDO and measure VDD\_LDO current and OUT\_LDO voltage. Fail the measure value which is not within limits.

Load Regulation: Calculate load regulation as given below and check for pass fail/limit.

$$\text{Load Regulation} = \frac{\text{LDO output at No load} - \text{LDO output at 11mA load}}{\text{LDO output at No load}} * 100$$

Line Regulation: Apply VDD\_LDO equal to 3.0V and measure OUT\_LDO voltage (VOUT1) with 11mA load current. Apply VDD\_LDO equal to 3.6V and measure OUT\_LDO voltage (VOUT2) with 11mA load current.

$$\text{Line Regulation} = \frac{\text{VOUT2} - \text{VOUT1}}{(3.6 - 3.0)} * 100$$

Check line regulation value for pass/fail limit.

**Offset Error Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set  $\text{OSR}=2048$  and  $f_{\text{MOD}} = 78.125 \text{ KHz}$ . Select analog channel 0 and PGA equal to 1.

Offset Error before Calibration: Apply 0V input. Read ADC data output and check for pass/fail limit.

Offset Error after self offset calibration: Perform self offset calibration. Read ADC output and checks the data for pass/fail limit.

Offset Error after system offset calibration: Perform system offset calibration. Read ADC output and check for pass/fail limit.

Repeat for all PGA setting.

**Full Scale Error Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set  $\text{OSR}=2048$  and  $f_{\text{MOD}} = 78.125 \text{ KHz}$ . Enable OLDD and OVDD. Select analog channel 0 and PGA equal to 1. Perform system offset calibration.

Full Scale Error before Calibration: Apply 2V at input. Read ADC data output and check for pass/fail limit.



Full Scale Error after self gain calibration: Perform self gain calibration. Apply 2V at input and read ADC output and checks the data for pass/fail limit.

Full Scale Error after system gain calibration: Apply 2V at input. Perform system gain calibration. Read ADC output and check for pass/fail limit.

Repeat for all PGA setting.

**CMRR (Common Mode Rejection Ratio) Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set OSR=2048 and  $f_{MOD} = 78.125$  KHz. Select analog channel 0 and PGA equal to 1. Perform system offset calibration. Short channel inputs INP and INN and apply input 0V to 3.3V ( $V_{CM}$ ) in step of 0.3V with reference to AGND. Read ADC data output for 20 samples at each step and record average value. Calculate the CMRR as given below.

$$CMRR = -20 * (\log_{10} ((|ADCOUT_0 - ADCOUT_{VCM}|) / V_{CM})) + (20 * (\log_{10} (PGA)))$$

Where  $ADCOUT_0$  is average value of ADC output at 0V input and  $ADCOUT_{VCM}$  is average value of ADC output at desire common mode input voltage. Check the calculated CMRR value for pass/fail limit. Repeat the procedure for all PGA setting.

**ENOB (Effective number of Bits) Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set  $f_{MOD} = f_{CLK} / 32$ . Select analog channel 0 and PGA equal to 1. Perform system offset and system gain calibration. Apply 1V at input and read ADC output for 100 samples at each PGA and OSR combinations. Calculate ENOB as given below.

$$ENOB\_NOS = 24 - \log_2 (ADCOUT_{MAX} - ADCOUT_{MIN}) + 2.7$$

Where  $ADCOUT_{MAX}$  and  $ADCOUT_{MIN}$  are maximum and minimum ADC output sample value. Check the calculated ENOB value for pass/fail limit.

**Missing Code Test (Histogram Method):** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set OSR=256 and  $f_{MOD} = 78.125$  KHz. Select analog channel 0 and PGA equal to 1. Perform system offset and system gain calibration. The sweep time of ramp signal for 14bit missing code verification can be calculated as follows:

$$\begin{aligned} ADC \text{ Update Rate} &= f_{MOD} / OSR = 78125 / 256 = 305.17578125 \text{ Hz} \\ Hits \text{ per Code} &= 5 \\ Sweep \text{ Time} &= 5 * 2^{14} / 305.17578125 = 268.435456 \text{ Seconds} \end{aligned}$$

Apply ramp signal varying from -2V to 2V of sweep time 269 second at input and read and dumped the ADC output for complete input signal. Process the dumped data for no. of hit obtained for 14 bit code. If 0 hit is found for any code mark the test as fail.

**DNL Test:** DNL is the difference in the expected hit count and obtained hit count normalized to an LSB. Ignore the zero and full scale code in the calculation. Calculate the DNL as follows.

$$DNL = (\text{hits obtained per code} / \text{average hit obtained per code}) - 1$$

Calculate the DNL at each code and check for pass fail limit.

**INL Test:** Calculate the INL as given below.

$$INL(n) = INL(n-1) + DNL(n) \quad \text{where } n \text{ is } 0, 1, 2, 3, \dots, 16383$$

Calculate the INL at each code and check for pass fail limit.