DATA SHEET

12-BIT,1MSPS, 7-CHANNEL SUCCESSIVE-APPROXIMATION-REGSITER (SAR)
ANALOG TO DIGITAL CONVERTER

SC1260-0T2

Version 1.0, October 2022

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PRODUCT DESCRIPTION:

The SC1260-0T2 device is a low-power; seven channel CMOS 12-bit Successive Approximation analog-to-digital converter specified for conversion throughput rates of 50kSPS to 1MSPS. The converter is based on successive approximation register architecture with an internal track-and-hold circuit. The device can be configured to accept up to seven input signals at inputs IN0 through IN6 and performs a 12-bit successive approximation analog-to-digital conversion in a nominal period of 16 clock cycles. The output serial data is straight binary and is compatible with serial interfaces. The 12-bit digital output has a tri-state control allowing the connection of multiple SC1260-0T2. This provides the ability to interface many sensor voltage readings to the digital processor data bus. The full-scale range is determined by analog supply voltages. The analog supply (V_A) can range from 3.0 V to 3.3V, and the digital supply (V_D) can range from 3.0 V to V_A. Normal power consumption using a 3.3V supply is < 20mW for 16MHz SCLK and <7mW for 1MHz SCLK.

FEATURES

- Resolution: 12Bits
- Sampling Frequency: 50KSPS to 1MSPS
- No missing code Guaranteed
- Output Data Format :Straight Binary
- Operating Voltage: 3.3V
- Power Consumption < 20mW for 16MHz SCLK and <7mW for 1MHz SCLK
- Input Range :3.3V Single Ended
- Package: 16 Lead Flat Package
- $Ø_{jc}$=7.1° C/W
- Technology: 180nm SCL CMOS Standard Logic Process

APPLICATIONS:

- Precision Sensors
- Motor Control
- High Temperature
- Medical Systems

BLOCK DIAGRAM:

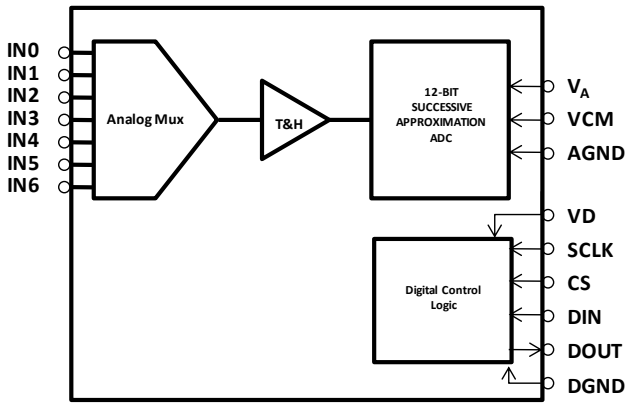

Figure 1: Device Block Diagram

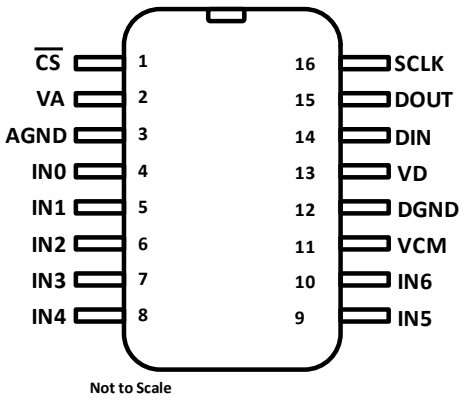

Figure-2: Pin Diagram

DEVICE SUMMARY:

Reference	Package	Pins	Lead Finish	Description	Junction Temp. range
SC1260-0T2	16 Lead Flat Package (16 Pin CFP)	16	Gold	Engineering Model	-55°C to +125°C

Table-1: Package Detail

Table-2: Pin Configuration

Pin No.	Pin Name	Pin Type	Pin Description
2	V_A	AP	Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet 3.3 V source and bypassed to GND with 1-µF and 0.1-µF monolithic ceramic capacitors located within 1 cm of the power pin.
13	V_D	DP	Positive digital supply pin. This pin should be connected to a 3.3 V to V_A supply, and bypassed to GND with a 0.1-µF monolithic ceramic capacitor located within 1 cm of the power pin.
3	AGND	Ground	The ground return for the analog supply and signals.
12	DGND	Ground	The ground return for the digital supply and signals.
1	$\overline{CS}$	DI	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
4,5,6,7,8,9,10	IN0 to IN6	AI	Analog inputs. These signals can range from 0 V to V_{REF}. IN0 to IN6 are for user inputs
11	VCM	Test Pin	Fixed for test input of $V_A/2$ with bypass capacitor of 1µf.
14	DIN	DI	Digital data input. The SC1260_0T2 Control Register is loaded through this pin on rising edges of the SCLK pin.
15	DOUT	DO	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
16	SCLK	DI	Digital clock input. The specified performance range of frequencies for this input is 0.8 MHz to 16MHz. This clock directly controls the conversion and readout processes.

- # PIN TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, AP = Analog Power, DP = Digital Power.

Table 3: RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Operating temperature	–55	25	125	°C
VA Supply voltage	3	3.3	3.63	V
VD Supply voltage	3	3.3	V_A	V
Digital input voltage	0	0	V_A	V
Analog input voltage	0	3.3	V_A	V
Clock frequency	0.05	1	16	MHz

ELECTRICAL SPECIFICATIONS:

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3V and Conversion rate =1MSPS unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

Table-4: Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
AVDD Analog supply voltage		2.97	3.3	3.63	V
DVDD Digital supply voltage		2.97	3.3	3.63	V
AVDD Operating current		1.10	1.14	1.18	mA
DVDD Operating current		0.91	1.08	1.19	mA
POWER DISSIPATION		6.67	7.35	7.85	mW
JUNCTION TEMPERATURE		-55	25	125	°C
DIGITAL INPUT					
VIH : Logic-high input voltage		2.0		DVDD	V
VIL : Logic-low input voltage		0		0.8	V
IIH : Logic-high input current		-10		10	µA
IIL : Logic-low input current		-10		10	µA
DIGITAL OUTPUT					
VOH : Logic-high output voltage	@5mA I_{OH}	3.24		3.3	V
VOL : Logic-low output voltage	@5mA I_{OL}	0		0.4	V
Output load capacitance	@1MHz		50		pF

ELECTRICAL SPECIFICATIONS (CONTINUED):

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Resolution			12	12	Bits
Conversion rate			50	1000	kSPS
Input Range			3.3		Vpp
No missing codes			Guaranteed		
Differential nonlinearity	CH0	-0.9		1.295	LSB
	CH1	-0.933		1.228	LSB
	CH2	-0.967		1.461	LSB
	CH3	-0.9		1.328	LSB
	CH4	-0.967		1.228	LSB
	CH5	-0.867		1.461	LSB
	CH6	-0.9		1.162	LSB
Integral nonlinearity	CH0	-1.327		3.238	LSB
	CH1	-1.505		2.086	LSB
	CH2	-1.704		2.209	LSB
	CH3	-1.627		2.136	LSB
	CH4	-1.677		3.159	LSB
	CH5	-1.7		3.196	LSB
	CH6	-1.732		3.256	LSB
Gain Error	CH0	0.372		0.427	% of FSR
	CH1	0.372		0.409	% of FSR
	CH2	0.372		0.403	% of FSR
	CH3	0.372		0.397	% of FSR
	CH4	0.348		0.415	% of FSR
	CH5	0.348		0.415	% of FSR
	CH6	0.354		0.421	% of FSR
Offset Error	CH0	-7.25		1	LSB
	CH1	-3.5		-0.75	LSB
	CH2	-3.5		-0.25	LSB
	CH3	-2		1	LSB
	CH4	-8		1.5	LSB
	CH5	-7.5		2	LSB
	CH6	-8.25		1	LSB
Input referred noise			< 1		LSB
Effective resolution			12		Bit
AC LINEARITY					
Signal To Noise Ratio (SNR)	Clock =1MHz Test Frequency = 1000.977Hz	68.51		70.07	dB
Total Harmonics Distortion (THD)		-74.19		-66.61	dB
Spurious-Free Dynamic Range (SFDR)		68.46		76.59	dB
Signal To Noise And Distortion (SINAD)		64.06		68.11	dB
ENOB		11.08		11.34	Bit

Table-5: Absolute Maximum Ratings*

Parameters	With respect To	Min.	Max.	Units
VA	Analog supply voltage	–0.3	3.6	V
VD	Digital supply voltage (2)	–0.3	V_A + 0.3	V
Voltage on any pin to GND		–0.3	V_A + 0.3	V
VIN	AVSS	-0.3	V_A + 0.3	V
DIGITAL INPUTS	AVSS	-0.3	V_A + 0.3	V
Input current at any pin (3)			±10	mA
Power dissipation T_A = 25°C			See (4)	
DIGITAL OUTPUTS	AGND	-0.3	DVDD	V
Storage Temperature		-65	150	ºC
Lead Temperature (10 Sec)			260	ºC
Junction temperature			125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions** are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum voltage is not to exceed 3.3V

(3) The absolute maximum junction temperature ($T_J$max) for this device is 125°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R\theta_{JA}$), and the ambient temperature (T_A), and can be calculated using the formula

$$P_D MAX = (T_J max - T_A)/R\theta_{JA}.$$

The values for maximum power dissipation listed above will be reached only when the SC1260_0T2 is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

SWITCHING SPECIFICATIONS

All typical specifications are at T_A = 25°C, all power supply voltages VA = VD = 3 V to 3.3 V, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} =50kSPS to 1 MSPS, and CL = 50pF, unless otherwise stated.

Table-6: **Typical timings for best performance with 1MSPS Conversion Rate**

Parameter	Description		MIN	NOM (1)	MAX	UNIT
t_{CSH}	$\overline{CS}$ hold time after SCLK rising edge	See (2)	10	0		ns
t_{CSS}	$\overline{CS}$ setup time prior to SCLK rising edge	See (2)	10	4.5		ns
t_{EN}	$\overline{CS}$ falling edge to DOUT enabled			5	30	ns
t_{DACC}	DOUT access time after SCLK falling edge			17	27	ns
t_{DHLD}	DOUT hold time after SCLK falling edge		7			ns
t_{DS}	DIN setup time prior to SCLK rising edge		10			ns
t_{DH}	DIN hold time after SCLK rising edge		10			ns
t_{CH}	SCLK high time			0.4 × t_{SCLK}		ns
t_{CL}	SCLK low time			0.4 × t_{SCLK}		ns
t_{DIS}	$\overline{CS}$ rising edge to DOUT high impedance	DOUT falling		2.4	20	ns
		DOUT rising		0.9	20	ns

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms.

(2) Clock may be in any state (high or low) when $\overline{CS}$ goes high. Setup and hold time restrictions apply only to $\overline{CS}$ going low.

Symbol	Parameter	Min	Typ	Max	Units
t_C	Conversion Rate	50KSPS	1MSPS		MSPS
$f_{SCLKMIN}$	Minimum clock frequency	0.8			MHz
$f_{SCLKMAX}$	Maximum clock frequency			16	MHz
t_{ACQ}	Acquisition (track) time			3	SCLK Cycles
$t_{CONVERT}$	Conversion (hold) time			13	SCLK Cycles
	Throughput time			16	SCLK Cycles

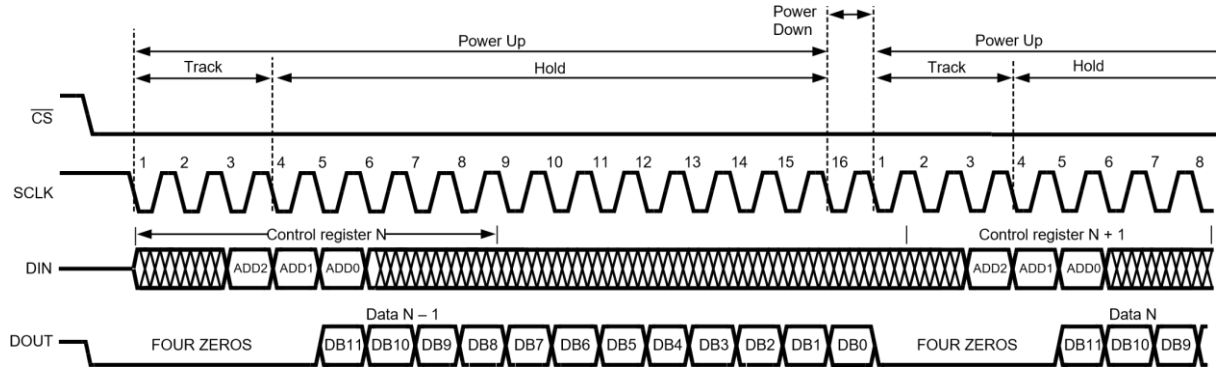

Figure 3: SC1260_0T2 Operational Timing Diagram

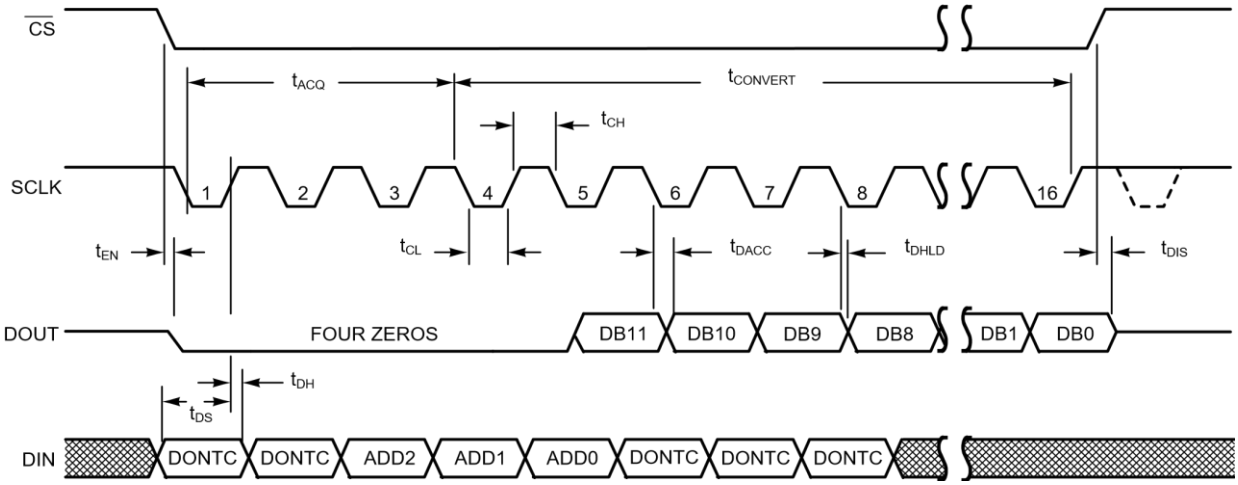

Figure 4: SC1260_0T2 Serial Timing Diagram

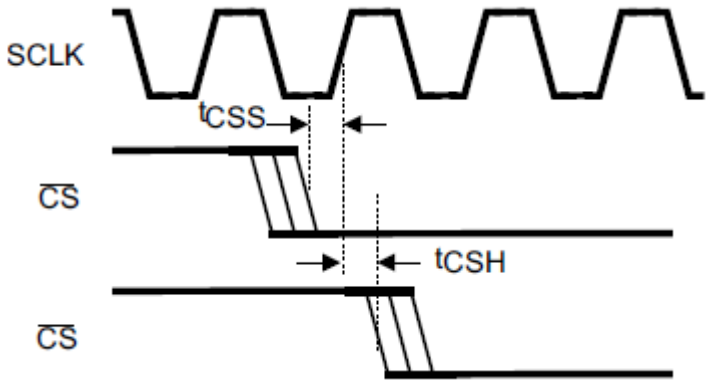

Figure 5: SCLK and CS Timing Parameters

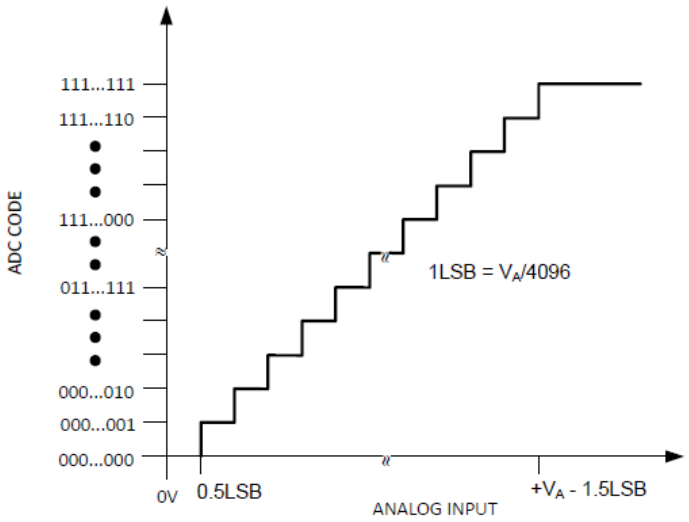

Figure 6: Ideal Transfer Characteristic

Table 7: Control Register Bit

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
DONTC	**DONTC**	**ADD2**	**ADD1**	**ADD0**	**DONTC**	**DONTC**	**DONTC**

Table 8: Control Register Bit Descriptions

BIT	SYMBOL	DESCRIPTION
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel will be sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in Table 9.
4	ADD1	
3	ADD0	

Table 9: Input Channel Selection

ADD2	ADD1	ADD0	INPUT CHANNEL
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6

TYPICAL CHARACTERISTICS:

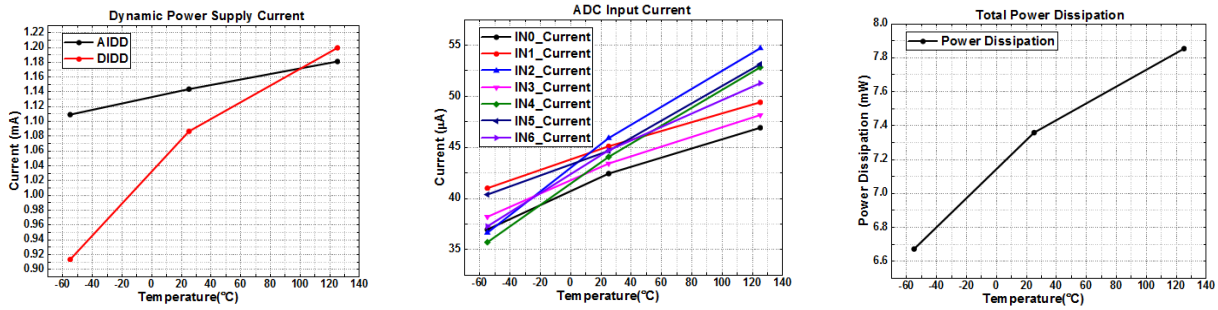

Figure 7: DC Characteristics

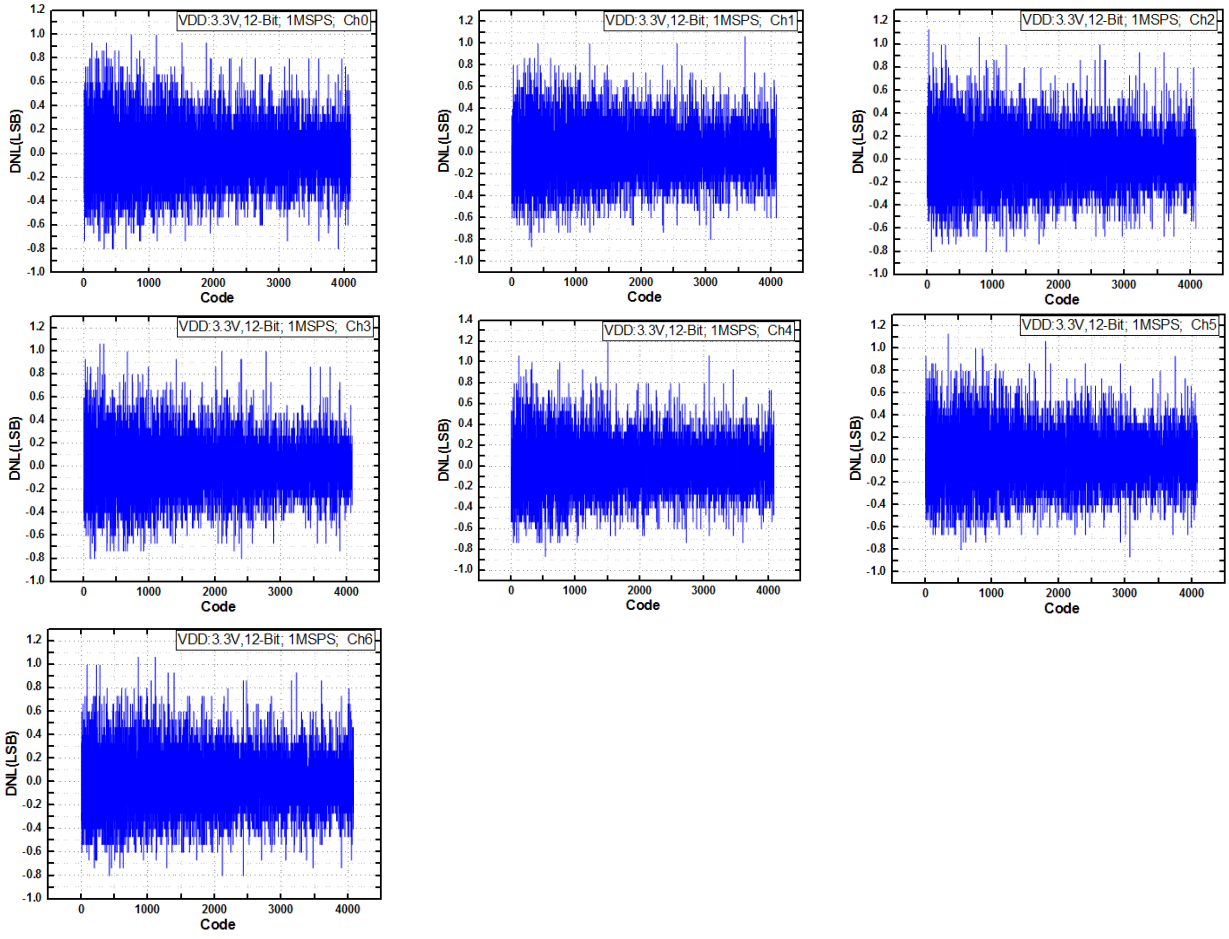

Figure 8: DNL Plots

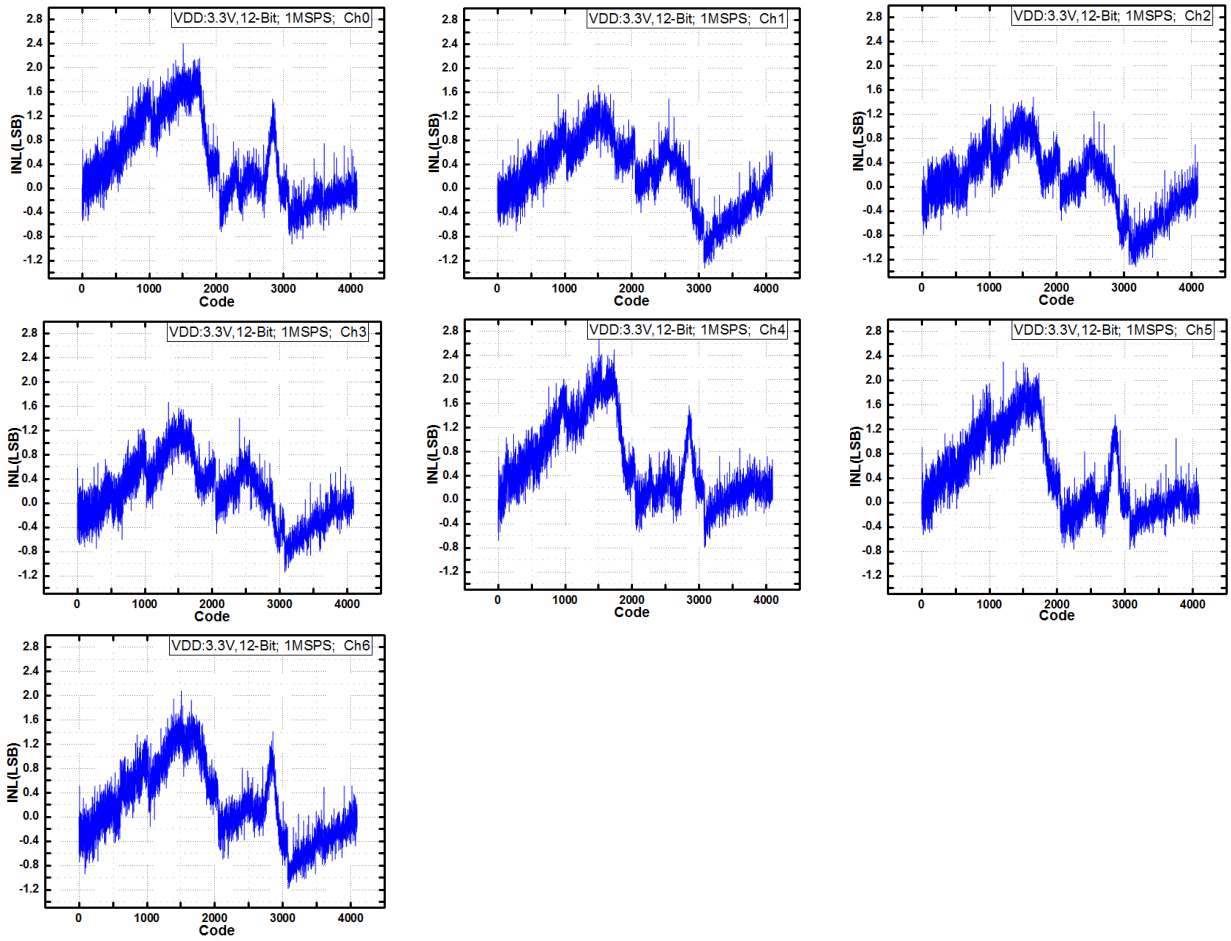

Figure 9: INL Plots

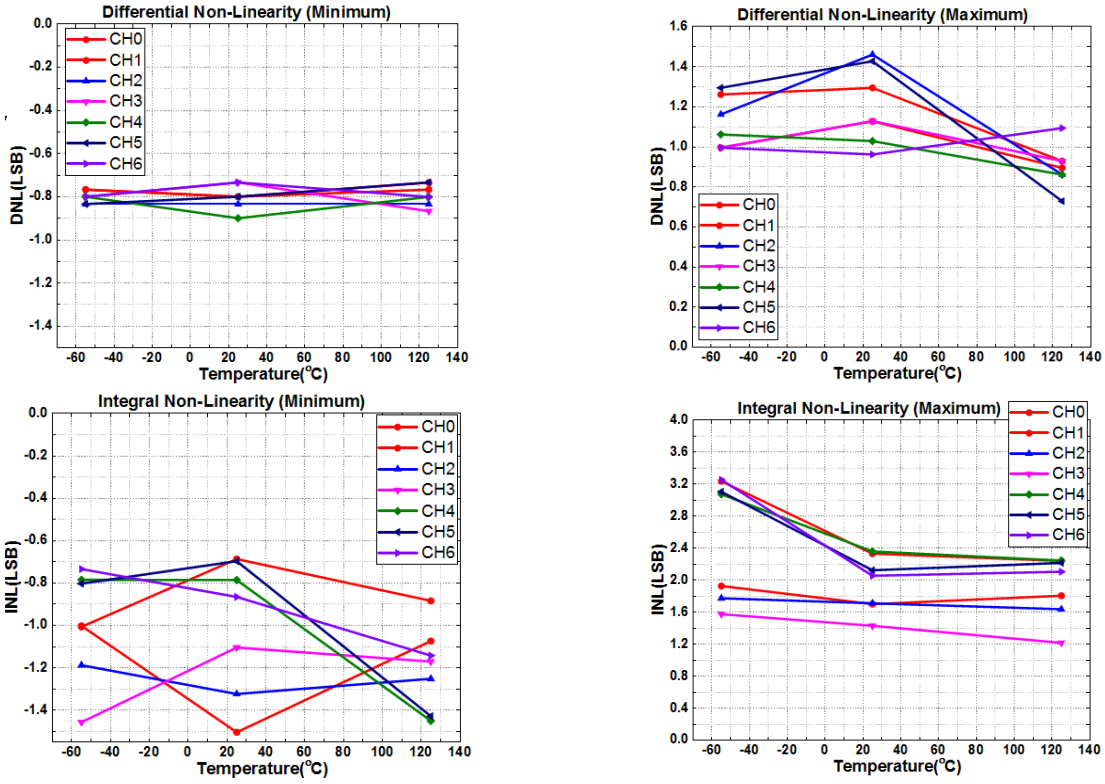

Figure 10: MAX-MIN DNL/INL Plots

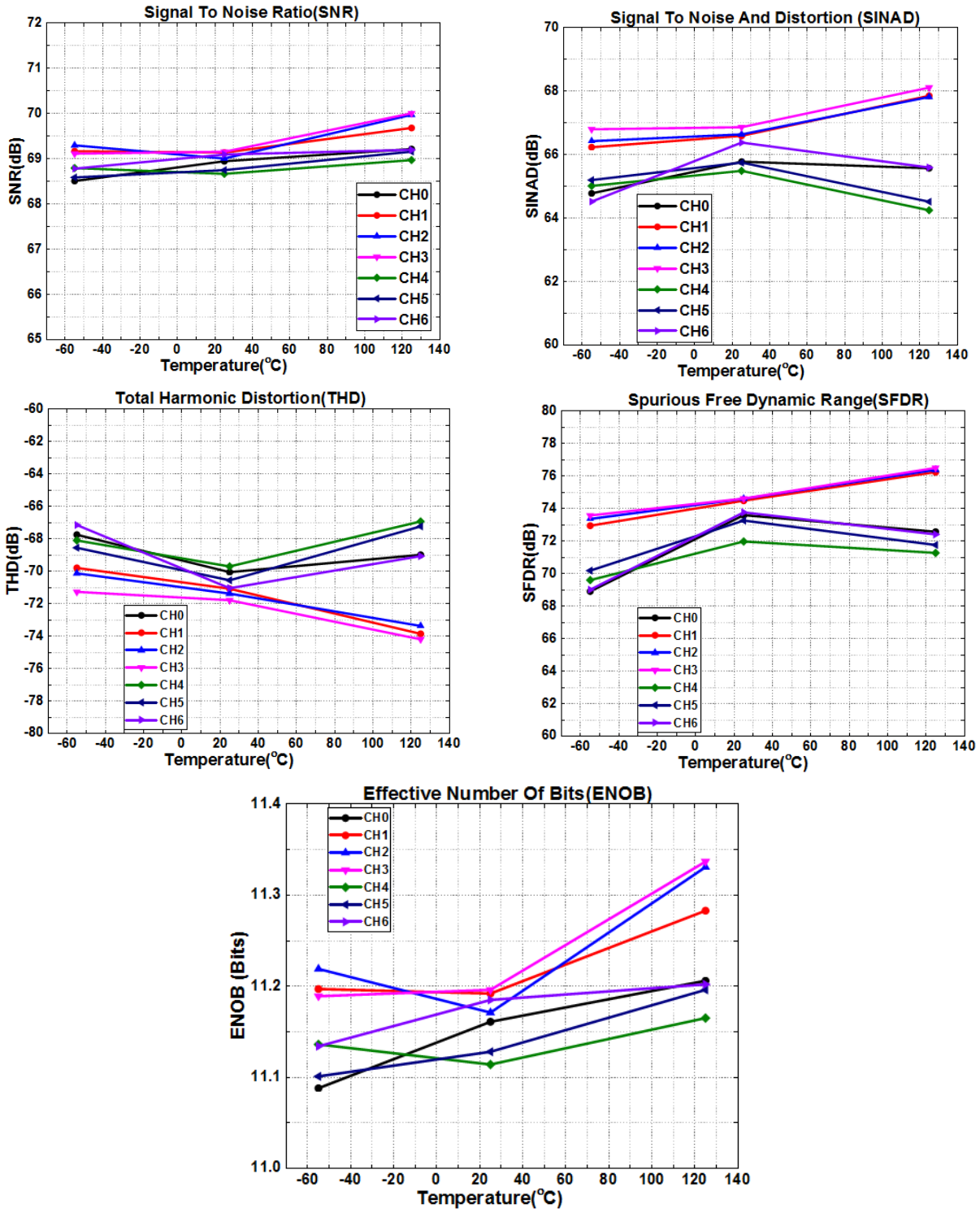

Figure 2: AC Plots

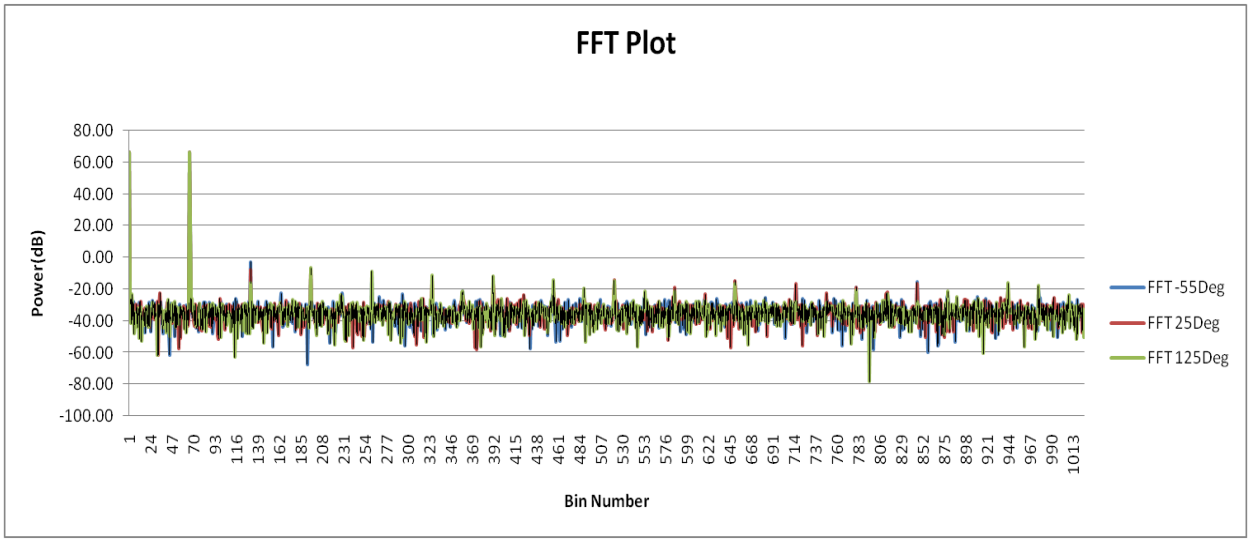

Figure 32: FFT Plots

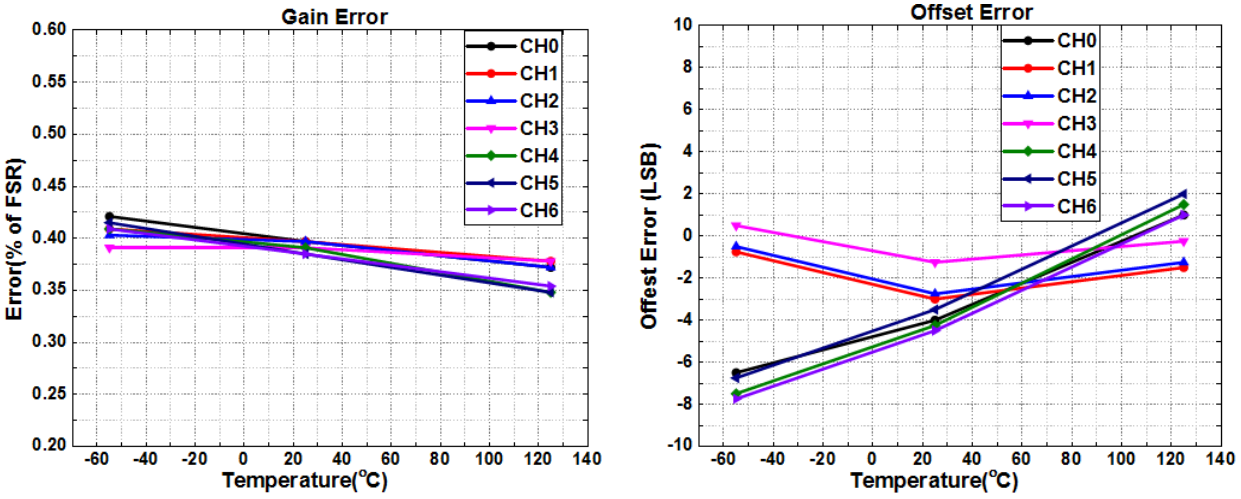

Figure 4: Gain and Offset Error

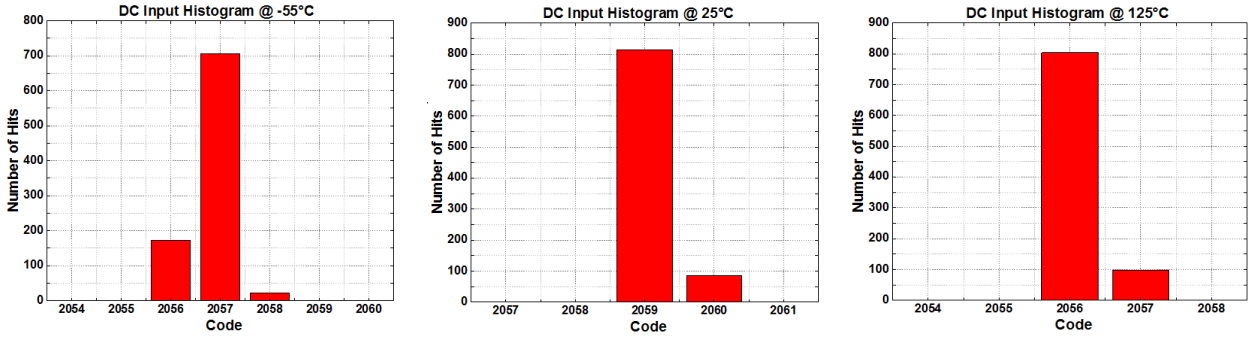

Figure 54: Histogram plot of output codes with analog grounded input (IN=1.65V)

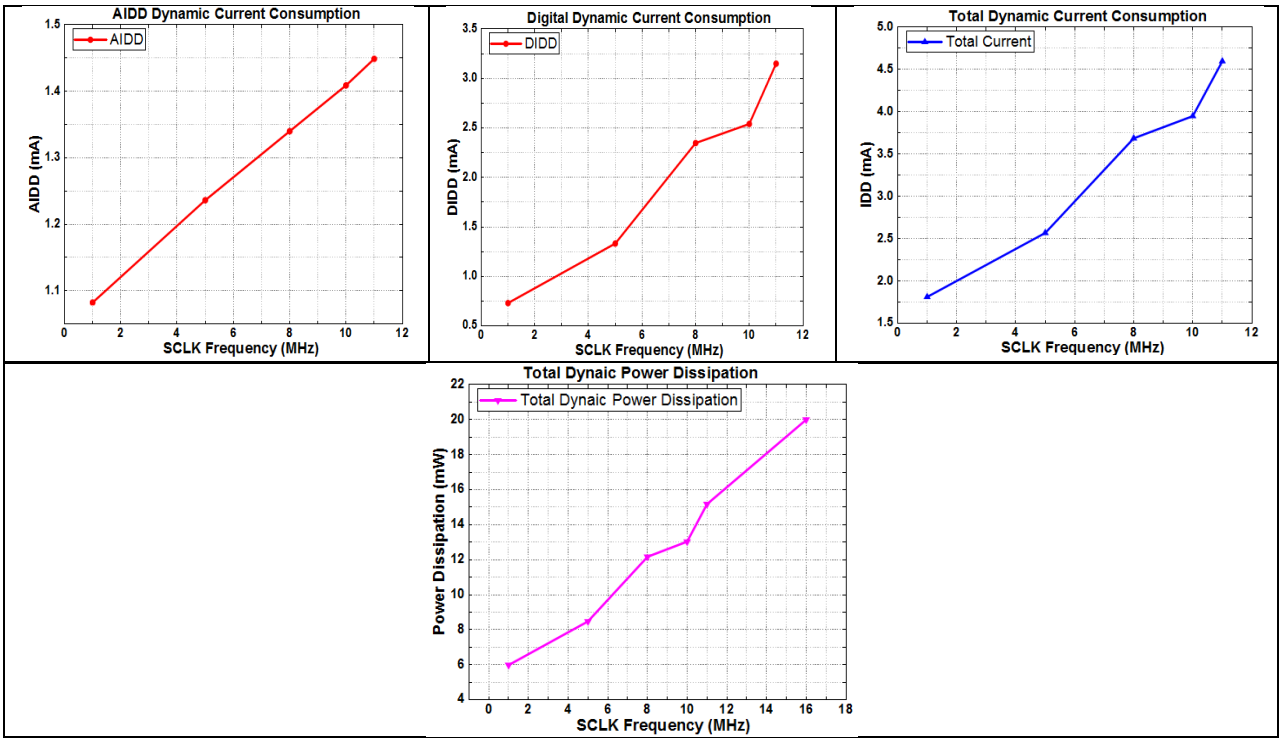

Figure *15*: Current Consumption and Power Dissipation at Different SCL frequency

OVERVIEW:

DEVICE DESCRIPTION

Overview

The SC1260_0T2 is a successive-approximation analog-to-digital converter designed around a charge redistribution digital-to-analog converter.

SC1260_0T2 Transfer Function

The output format of the SC1260_0T2 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the SC1260_0T2 is V_A / 4096. The ideal transfer characteristic is shown in Figure 6. The transition from an output code of 000000000000 to a code of 000000000001 is at 1/2 LSB, or a voltage of V_A / 4096. Other code transitions occur at steps of one LSB.

Serial Interface Programming

An operational timing diagram and a serial interface timing diagram for the SC1260_0T2 are shown in Figure 3 to Figure 5. $\overline{CS}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the SC1260_0T2's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion. A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when is high and is active when $\overline{CS}$ is low. Note that $\overline{CS}$ is asynchronous. Thus, $\overline{CS}$ acts as an output enable. During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out. SCLK falling edges 1 through 4 clocks out leading zeros while falling edges 5 through 16 clocks out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the hold/convert mode on the N×16+4th falling edge of SCLK. "N" is an integer value. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, see Figure 3 for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK. During each conversion, data is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. The control register is loaded with data indicating the input channel to be converted on the subsequent conversion (see Table 7, Table 8, and Table 9). Although the SC1260_0T2 is able to acquire the input signal to full resolution in the first conversion immediately following power-up, the first conversion result after power-up will be that of a randomly selected channel. Therefore, the user needs to incorporate a dummy conversion to set the required channel that will be used on the subsequent conversion.

Definitions of Specification

TOTAL OUTPUT NOISE

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain . The output noise can be converted to an equivalent voltage, using the relationship

$$1\ \text{LSB} = (\text{ADC full scale} / 2^N\ \text{codes})$$

Where N is resolution of the ADC. 1 LSB is approximately 805μV.

EFFECTIVE RESOLUTION

The ratio of the full-scale input range to the rms input noise (from grounded input histogram test) is called as effective resolution.

$$\text{Effective resolution} = \log_2\left(\frac{2^N}{\text{rms input noise (LSBs)}}\right)$$

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicate that all 4096 codes, respectively, must be present overall operating ranges.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

N = (SINAD – 1.76)/6.02

It is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

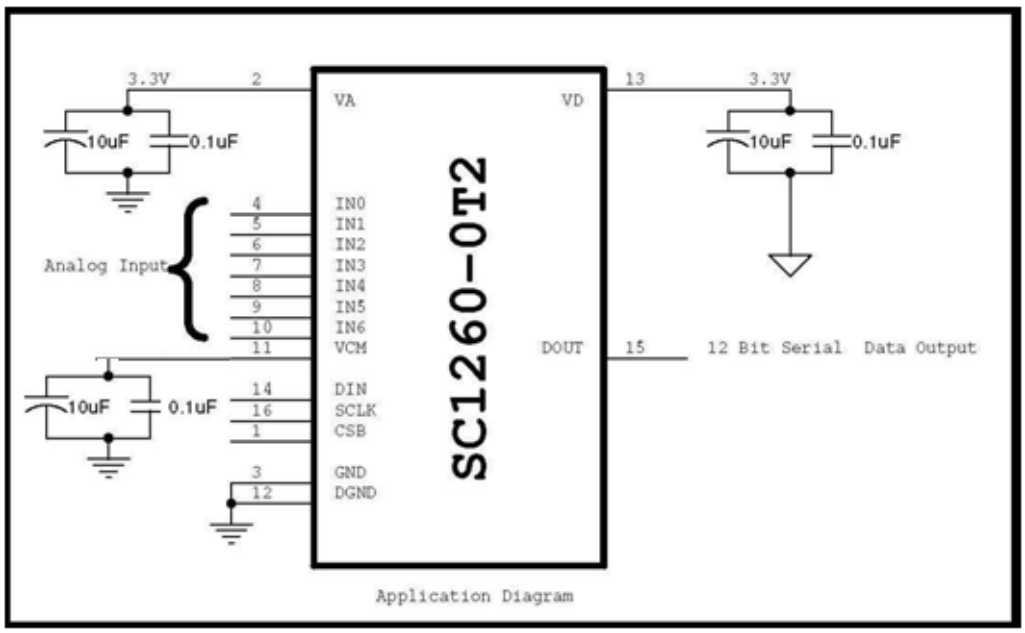

Figure-16: Application Diagram

PACKAGE DRAWING (16 Pin CFP):

Note7: All linear dimensions are in inches (mm.)

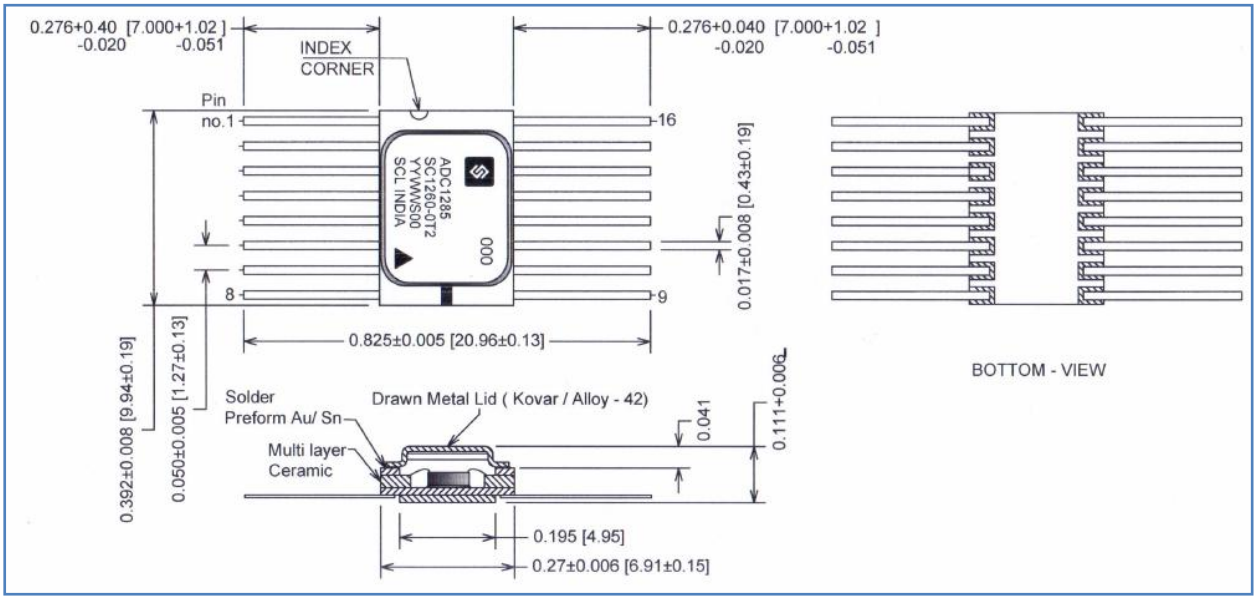

Figure-17: Package Drawing

Revision History			
S.No.	**Version**	**Date of release**	**Description**
1	1.0	October 20, 2022	
2			
3			
4			

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