SC9041-0S

December 2024

PRELIMINARY DATASHEET

16 Bit Cyclic-ADC (CADC)

FEATURES

- 16-Bit 500Ksps ADC
- Low Power: 100 mW at 500Ksps
- On -Chip Reference and Track/Hold
- SNR> 65dB
- 2V p-p Analog Input Range
- Single 3.3V Supply Operation
- ESD Protection >1KV HBM
- Package: 64 Pin CQFP
- Technology: 0.18um SCL CMOS Standard Logic Process
- Temperature Range: -55ºC to +125ºC.
- θ_{JC}:3.7°C/W

APPLICATIONS

- Battery Powered Instruments
- Instrumentation Electronics
- Sensor Applications

DESCRIPTION

The 16-bit 500KSPS CADC is a monolithic CMOS Cyclic Analog-to-Digital Converter capable of converting analog input signals into 16-bit digital word at 500 Kilo samples per second (KSPS) and designed for battery powered low power instrumentation and imaging applications. This converter uses a differential cyclic architecture. Operating on a single 3.3V power supply, device achieves ≥ 13-bits effective resolution at nyquist rate and consumes < 100mW. The Power Down feature reduces power consumption to <15mW. The differential inputs provide a full scale differential input swing equal to 4 times of V_{REF} (4*(CAPTE-CAPBE)). Full scale input range is recommended for optimum performance. The ASIC is fabricated in 0.18µm SCL CMOS Standard Logic Process.

Table 1 Device Summary

Reference	Package	Pins	Lead Finish	Temp. Range
SC9041_0S	CQFN	64	Gold	-55ºC to 125ºC

BLOCK DIAGRAM

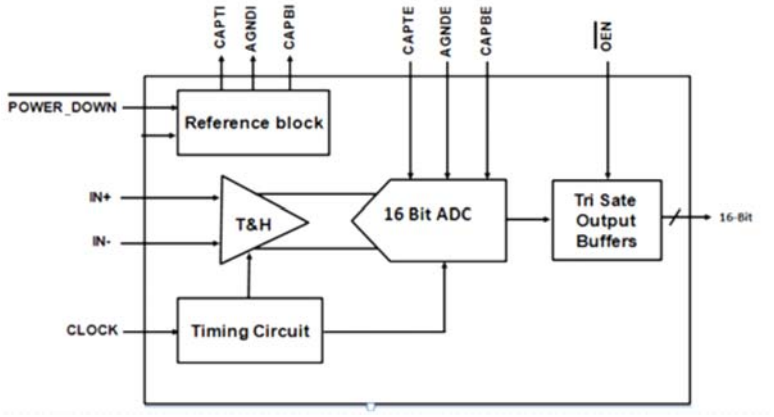

Figure 1: Block Diagram of a SC9041_0S

PIN CONFIGURATION

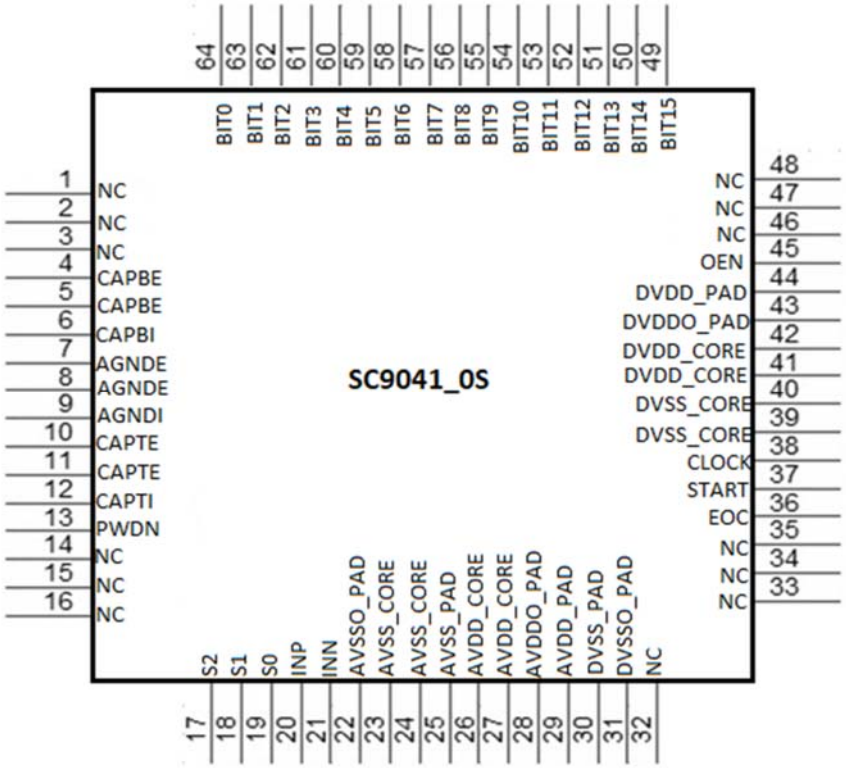

Figure 2: Device Pin Diagram

PIN DESCRIPTION

Table 2: Pin Description of SC9041_0S

Pin No	Name	Pin Type	Description/Remarks
1-3	NC		No Connection
4	CAPBE	AO	External ADC Bottom Reference Voltage
5	CAPBE	AO	External ADC Bottom Reference Voltage
6	CAPBI	AI	Internal ADC Bottom Reference Voltage
7	AGNDE	AO	External common mode Analog Ground
8	AGNDE	AO	External common mode Analog Ground
9	AGNDI	AI	Internal common mode Analog Ground
10	CAPTE	AO	External ADC Top Reference Voltage
11	CAPTE	AO	External ADC Top Reference Voltage
12	CAPTI	AI	Internal ADC Top Reference Voltage
13	PWDN	DI	Power Down PIN (Active Low)
14-16	NC		No Connection
17	S2	DI	Power Selection test pin (0V/3.3V)
18	S1	DI	Power Selection test pin (0V/3.3V)
19	S0	DI	Power Selection test pin (0V/3.3V)
20	INP	AI	ADC IN+
21	INN	AI	ADC IN-
22	AVSSO_PAD	AP	Analog Negative Supply (0 V)
23	AVSS_CORE	AP	Analog Negative Supply (0 V)
24	AVSS_CORE	AP	Analog Negative Supply (0 V)
25	AVSS_PAD	AP	Analog Negative Supply (0 V)
26	AVDD_CORE	AP	Analog Positive Supply (+3.3 V)
27	AVDD_CORE	AP	Analog Positive Supply (+3.3 V)
28	AVDDO_PAD	AP	Analog Positive Supply (+3.3 V)
29	AVDD_PAD	AP	Analog Positive Supply (+3.3 V)
30	DVSS_PAD	DP	Digital Negative Supply (0 V)
31	DVSSO_PAD	DP	Digital Negative Supply (0 V)
32-35	NC		No Connection
36	EOC	DO	End of Conversion
37	START	DI	Start of Conversion
38	CLOCK	DI	ADC Clock

Pin No	Name		Description/Remarks
39	DVSS_CORE	DP	Digital Negative Supply (0 V)
40	DVSS_CORE	DP	Digital Negative Supply (0 V)
41	DVDD_CORE	DP	Digital positive Supply (3.3 V)
42	DVDD_CORE	DP	Digital positive Supply (3.3 V)
43	DVDDO_PAD	DP	Digital positive Supply (3.3 V)
44	DVDD_PAD	DP	Digital positive Supply (3.3 V)
45	OEN	DI	Output enable (Active Low)
46-48	NC		No Connection
49	BIT15	DO	ADC digital output Bit (MSB)
50	BIT14	DO	ADC digital output Bit
51	BIT13	DO	ADC digital output Bit
52	BIT12	DO	ADC digital output Bit
53	BIT11	DO	ADC digital output Bit
54	BIT10	DO	ADC digital output Bit
55	BIT9	DO	ADC digital output Bit
56	BIT8	DO	ADC digital output Bit
57	BIT7	DO	ADC digital output Bit
58	BIT6	DO	ADC digital output Bit
59	BIT5	DO	ADC digital output Bit
60	BIT4	DO	ADC digital output Bit
61	BIT3	DO	ADC digital output Bit
62	BIT2	DO	ADC digital output Bit
63	BIT1	DO	ADC digital output Bit
64	BIT0	DO	ADC digital output Bit (LSB)

ABSOLUTE MAXIMUM RATING

Table 2: Absolute Maximum Rating*

Parameter	With respect to	Min.	Max.	Unit
INP, INN, CAPTE, CAPBE,AGNDE	AVSS	-0.3	AVDD + 0.3	V
Digital Inputs	AVSS	-0.3	AVDD + 0.3	V
AVDD	AVSS	-0.3	4.3	V
DVDD	DRVSS	-0.3	4.3	V
AVSS	DRVSS	-0.3	0.3	V
Digital Outputs	DRVSS	-0.3	DRVDD +0.3	V
Storage Temperature		-65	150	°C
Lead Temperature (10 Sec)			300	°C

ESD Tolerance (HBM)			>1000	V
Latch Up Protection			100	mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
AVDD	Analog Positive Supply	3.135	3.3	3.465	V
DVDD	Digital Power Supply	3.135	3.3	3.465	V
V_{IH}	High level input voltage	2.0	-	DVDD	V
V_{IL}	Low level input voltage	DVSS	-	0.8	V
V_{OH}	High level output voltage	2.4	-	DVDD	V
V_{OL}	Low level output voltage	DVSS		0.8	V
T_A	Ambient temperature range	-55	-	+125	ºC

ELECTRICAL CHARACTERISTICS

All typical specifications are at Temp = -55 to 125°C, all power supply voltages = 3.3V, and conversion rate 500KSPS, unless otherwise stated.

Table 4: Electrical characteristics of SC9041_0S

Parameters	Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
AVDD Analog Supply Voltage		3.135	3.3	3.465	V
DVDD Analog Supply Voltage		3.135	3.3	3.465	V
AVDD Operating Current	S2:S0 = 0	3	9	12	mA
	S2:S0 = 1	6	12	15	mA
	S2:S0 = 2	9	15	18	mA
	S2:S0 = 3	12	18	21	mA
	S2:S0 = 4	15	21	24	mA
	S2:S0 = 5	18	24	27	mA
	S2:S0 = 6	21	27	30	mA
	S2:S0 = 7	24	30	33	mA
DVDD Operating Current	S2:S0 = 0 to 7	2.3	2.6	2.9	mA
EXTERNAL REFERENCE					
Positive Reference Voltage	CAPTE		1.9		V
Negative Reference Voltage	CAPBE		1.4		V
Common Mode Voltage	AGNDE		1.65		V
CURRENT REQUIREMENT					
Positive Reference Voltage	CAPTE			150	uA
Negative Reference Voltage	CAPBE			150	uA

Common Mode Voltage	AGNDE			1	mA
INTERNAL REFERENCE					
Positive Reference Voltage	CAPTI	1.971		2.013	V
Negative Reference Voltage	CAPBI	1.425		1.458	V
Common Mode Voltage	AGNDI	1.675		1.710	V
Temperature Drift	CAPTI			150	ppm/°C
	CAPBI			100	ppm/°C
	AGNDI			150	ppm/°C
DIGITAL INPUT					
VIH : Logic-high input voltage		2.0		DVDD	V
VIL : Logic-low input voltage		0		0.8	V
IIH : Logic-high input current		-10	1	10	uA
IIL : Logic-low input current		-10	1	10	uA
Input capacitance			5		pF
DIGITAL OUTPUT					
VOH : Logic-high output voltage	@100 µA IOH	2.4	3.28	3.3	V
VOL : Logic-low output voltage	@100 µA IOL	0	0.06	0.4	V
Output load capacitance			10		pF
FUNCTIONAL SPECIFICATIONS					
Resolution				16	Bits
No missing codes[#]			Guaranteed		
Conversion Rate				500	KSPS
Input Range			2		Vp-p
CMRR		45			dB
PSRR		65			dB
Effective Resolution (ENOB)		13.4			Bits
Differential Non-Linearity (DNL)		-0.7		0.9	LSB
Integral Non-Linearity (INL)		-28		3	LSB
Offset Error				100	LSB
Full Scale Range Error (FSR Error)				100	LSB
Gain Error		-0.2		0.2	%
DYNAMIC PARAMETERS					
Signal to Noise Ratio (SNR)	F_{in} = 3.2KHz F_s = 400KSPS	64			dB
Total Harmonics Distortion (THD)				-67	dB
Signal to Noise and Distortion (SINAD)		63			dB

No missing codes are verified and tested up to 14 bits

DEVICE OVERVIEW

SC9041-0S is a low-power fully differential cyclic analog-to-digital converter (ADC) for sensors processing electronics and image sensor readout circuits. The Cyclic ADC with redundant signed digital (RSD) algorithm has advantages, such as simpler circuit configuration and more tolerance to offset error of comparator. CADC is the combination of pipelined and SAR ADC.

Figure 2 shows a block diagram of a cyclic analog-to-digital converter. The architecture contains one sample-and-hold (S/H) stage to sample the input or the residue signal from the previous step. This residue signal is generated according to the decision outputs of the comparator, and the gain stage is used to amplify the residue signal to reuse the full-scale reference voltage. The cyclic ADC performs this analog-to-digital conversion recursively. Therefore, it requires a less analog circuitry and achieves the most area-efficient design of any type of ADC.

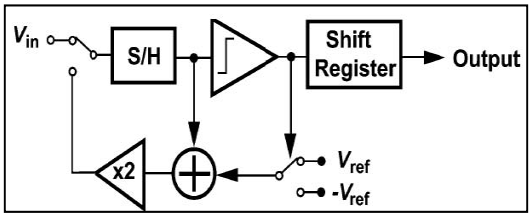

Figure 2 General block Diagram of a Cyclic ADC

Three State Output

The digital outputs of the SC9041_0S can be placed in a high impedance state by setting $\overline{OEN}$ signal HIGH.

Reference Voltages

SC9041_0S features in-built internal reference voltages. To use internal reference voltages, CAPTI, AGNDI and CAPBI pins should be connected to CAPTE, AGNDE and CAPBE, respectively. Depending on the application requirements it might be advantageous to operate the ADC with an external reference voltage. This will improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy.

Power Down Mode

SC9041_0S can be placed in power down mode by setting POWER_DOWN signal low. If POWER_DOWN signal is low, complete chip will be in power down mode except voltage reference. To make complete chip in power down POWER_DOWN should be connected to DVSS.

TIMING RELATIONS

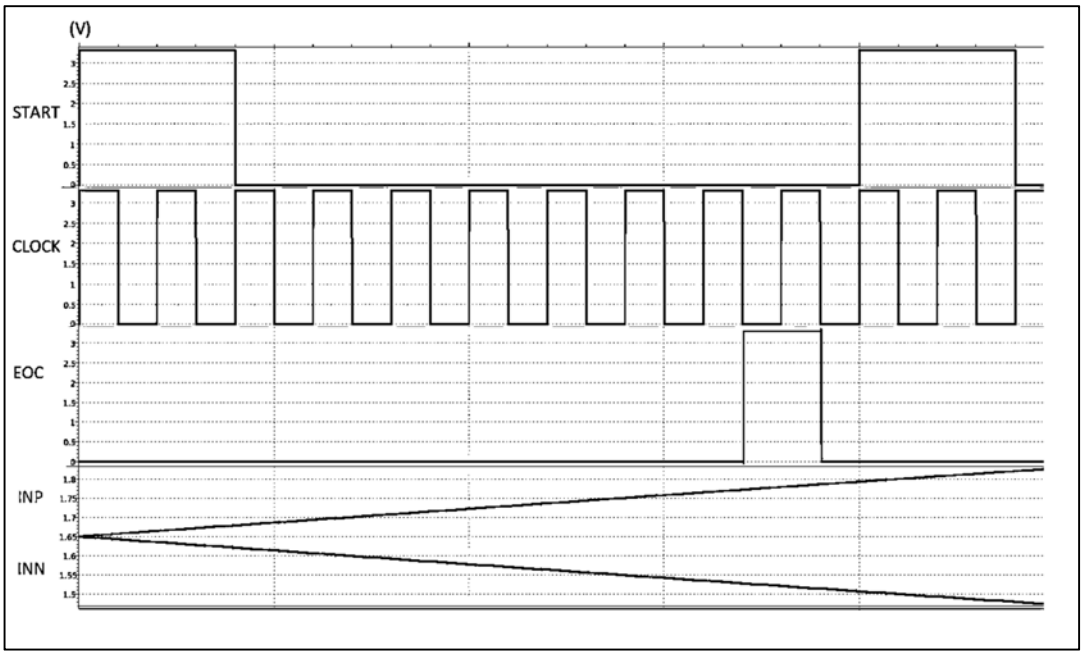

Figure 3 Timing Relations of SC9041_0S

TYPICAL CHARACTERISTICS

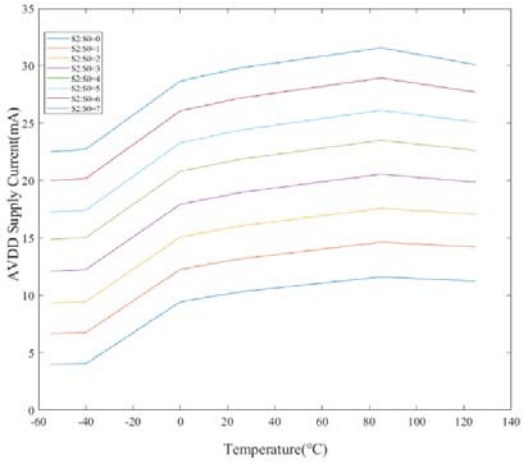

Figure 4 AVDD Supply Current vs Temperature

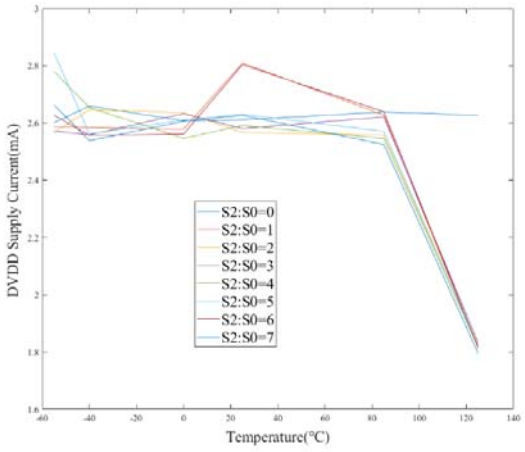

Figure 5 DVDD Supply Current vs Temperature

DEFINITIONS OF KEY PECIFICATIONS

Differential Non-Linearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 16-bit resolution indicate that all 65536 codes must be present overall operating conditions.

Integral Non-Linearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level $1\frac{1}{2}$ LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of ADC output codes is measured in LSB and represents the rms noise level of the total signal chain. The output noise can be converted to an equivalent voltage, using the relationship

1 LSB = (ADC full scale / 2^N codes)

Where N is resolution of the ADC. 1 LSB is approximately 30uV.

Effective Resolution

The ratio of full scale input range to the rms input noise (from grounded input histogram test) is called as effective resolution.

$$\text{Effective Resolution} = \log_2\left(\frac{2^N}{(rms\ input\ noise\ (LSBs))}\right)$$

Where N is resolution of the ADC.

PACKAGE INFORMATION

Figure 15: SC9041_0S in 64 Pin CQFP

All dimensions are in mm unless specified

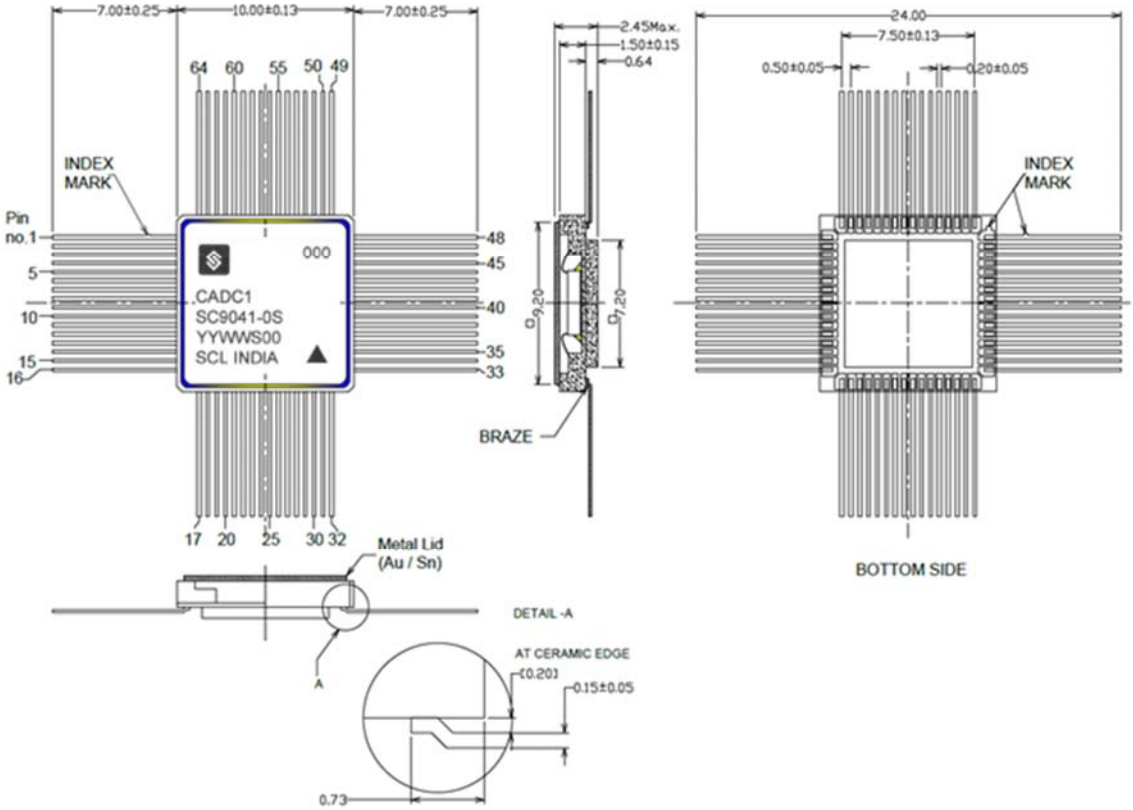

Figure 16: Package Drawing

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