B. Research Areas in CMOS Process Technology

B.1	**Radiation Hardened 1.8V/3.3V/5.0V I/O PAD development for SCL's 180nm Technology** 1. I/O pad for analog signals 2. Power Pads for VDD, VSS, VSUB 3. Power Clamp VDD- VSS, VDD- VSUB , VSS-VSUB 4. Power Clamp for I/O. ESD > 2kV HBM, Latch up immunity ± 100 mA, (Tj=125 ^{0}C), PAD Size =65x250 um, Radiation Tolerance : TID >300 krad(Si) SEL > 50 Mev-cm^2/mg SEU > 50 Mev-cm^2/mg
B.2	**20 V I/O PAD development for SCL's 180nm Technology** 1. I/O pad for analog signals 2. Power Pads for VDD, VSS, VSUB 3. Power Clamp VDD- VSS, VDD- VSUB , VSS-VSUB 4. Power Clamp for I/O. Operating Voltage 20V, Abs. Max. rating >24V, ESD > 2kV HBM, Latch up immunity ± 100 mA (Tj=125 ^{0}C), PAD Size =65x250 um.
B.3	**Design/PDK enablement of new devices in SCL's 180nm CMOS process** Any new device developed in SCL process need to be enabled inside existing IC design EDA flow supported by SCL technology. This enables design engineer to use these new devices in their designs using standard IC design EDA tools. EDA flow used for designing with SCL CMOS technology is primarily based on EDA softwares. Software files need to be developed for various IC design elements while working with EDA tools. Following IC design elements are part of PDK library: Device symbols, CDF parameters, SKILL codes, Layout

	programmable cells (PCELLs), DRC, LVS, PEX verification rule decks. Software files need to be developed for these design elements for any device which needs to be integrated inside IC design flow. Skill set required for this work is good knowledge of EDA software programming along with background knowledge in semiconductor and IC domain.
B.4	**Radiation Hardened 20V I/O PAD development for SCL's 180nm Technology** 1. I/O pad for analog signals 2. Power Pads for VDD, VSS, VSUB 3. Power Clamp VDD- VSS, VDD- VSUB , VSS-VSUB 4. Power Clamp for I/O. Operating Voltage 20V, Abs. Max. rating >22V, ESD > 2kV HBM, Latch up immunity ± 100 mA (Tj=125 ^{0}C), PAD Size =65x250 um, Radiation Tolerance : TID >300 krad(Si) SEL > 50 Mev-cm^{2}/mg SEU > 50 Mev-cm^{2}/mg
B.5	**Technology Development of High Power RF LDMOS Device** SCL has initiated in-house development of high Power RF LDMOS devices. In this work development of two different RF LDMOS devices for 650MHz (~500Watt) and 325MHz (1kWatt) operations has been initially targeted. In this regard SCL requires support for following topics: 1. Device Design for state of the art and reliable, rugged High voltage (~50V) RFLDMOS. 2. Process & Implant conditions (must be supported with TCAD simulated results). 3. Test chip for RF LDMOS process integration 4. RF characterization and Reliability analysis of developed devices.

B.6	**Modeling of HV (10, 20, 40, 50/60V) devices (N and P MOS)** Process development work at SCL is in progress for the process integration of LDMOS (VDS: 10-20, 40-60V; VGS: 3.3-5V) devices (n and PMOS) in standard 180nm baseline process. Once the devices are enabled, SPICE device models are required for the above LDMOS devices for circuit design implementation. The developed models should be accurately predicting both DC and AC performance of the devices over a range of voltage, temperatures (-55 to 125C) and frequencies. Deliverables: i. Device characterization (DC-IV, CV, RF) as required for Model parameter extraction. ii. Industry standard LDMOS Device Models (Scalable /Binned) Model QA report complying IEEE/CMC model validation tests and accuracy.
B.7	**PDK Development for HV Process**
B.8	**Modelling of Devices in SOI-CMOS Process**
B.9	**Enablement of PDK for HV, Bipolar and SOI CMOS Process**
B.10	**Studies on epitaxial growth and characterization of lattice matched InAlN/GaN Heterostructures on silicon for high power applications** GaN-based wide band gap semiconductors are suitable for light emitting diodes, solar cells and ultraviolet photodiodes applications. They are also of use for wireless network base stations and satellite communication systems etc. where GaN-based devices can multiply the efficiency of amplifiers. However, improvements in GaN-based High Electron Mobility Transistors (HEMTs) are limited by the fundamental parameters of established AlGaN / GaN heterostructures. The objective is to explore new heterostructures using InAlN/GaN alloys and enhance the potential power density of HEMTs. InAlN alloys are attractive due to their wide bandgap (0.6 to 6.2 eV) and lattice matching capability with GaN. Extremely high electron gas density coupled with polarization fields in the heterojunction

	offers power densities of 30W/mm at 2 to 12 GHz. Focus should be on optimizing the growth of InAlN/GaN HEMT layers on Si using metalorganic vapour deposition (MOCVD) techniques to demonstrate high performance HEMT devices.
B.11	**Development of Gallium Nitride-based Ultraviolet (UV) photodetectors on Silicon:** Conventional silicon-based UV detectors have some major intrinsic limitations such as aging due to exposure to radiation of much higher energy than the Si bandgap, reduced quantum efficiency in the deep-UV range, significant loss of effective area due to the need to use filters and cooling if low dark current is required. On the other hand, Group III Nitrides offer advantages over Si for UV detection. It is proposed to develop GaN-based ultraviolet (UV) detectors on Si with high performance. GaN and AlGaN layer structures of appropriate composition are required to be grown on Si substrates using MOCVD. Structural, electrical and optical characterizations need to be carried out to optimize the quality, composition and thickness of the layers suitable for photodetector applications. The (Al)GaN MSM (metal-semiconductor-metal) UV detectors (<280 nm) need to be designed and fabricated. The fabricated GaN/Si UV detectors will be aimed to exhibit high performance such as low dark current and high responsivity. Further studies may include addressing the dark current issues using insulating layers such as ZrO2 and HfO2.
B.12	**Development of process technology for Germanium–via heterogeneous integration with silicon:** It is required to develop a growth method of Ge on Si integration using Chemical Vapour Deposition (CVD) with the aim to achieve reasonable quality for electronic and photonic applications. Once the Ge/Si hetrostructure with the desired properties is obtained, it is required that their electrical and optical properties need to be studied by fabricating active devices. The proposed development work should cover materials study, growth/fabrication, and device characterization.

B.13	**Development of Dry Etch Technology for Aluminum Free InGaP/GaAs/InGaAs epitaxial films for Laser Diodes**: Aluminum Free InGaP/GaAs/InGaAs laser diodes are receiving a great deal of attention because of their superior performance and reliability in comparison to more conventional AlGaAs/GaAs/InGaAs laser diodes. Interest in these devices is driven by their compatibility with the epitaxy-on-electronics (EoE) monolithic optoelectronic integration technology. In particular, high quality aluminum-free laser diodes can be grown at temperature below 475°C, which are compatible with EoE technology whereas laser diodes with aluminum in or near their active regions cannot be grown at such low temperatures. An important challenge with aluminum-free hetrostructures is dry etching vertical end mirror facets and angled deflector structures because of the very different chemical makeup of the layers. In particular, the wider bandgap InGaAsP layers contain significant amounts of In and P, and relatively little or no As, whereas the narrow gap GaAs and InGaAs layers contain roughly 50% As no P, and relatively little or no In. Conventional chlorine based and methane based dry etch techniques do not work well with the Aluminum free hetrostructures. Literature suggest that ion bean assisted chlorine etching of InGaP is very slow at room temperature; at elevated temperature where InGaP etch satisfactorily, GaAs layer are etched without ion beam and several lateral etching occurs, i.e. the etch is not directional and anisotropic. The solution to this problem lies in changing the etchant from chlorine to bromine because the vapour pressures of the relevant bromides are much more similar than are those of corresponding chlorides. Consequently, it is possible to find etch conditions for which the etch rates of InGAP and GaAs are sufficiently similar that vertical mirror facets can be successfully etched. Therefore, it is proposed to develop an etch chemistry for the aforesaid application.
B.14	**Si-on-GaAs: Monolithic Hetrogenous Integration of Si-CMOS with GaAs Optoelectronic Devices using EoE technology:** As electronic technology becomes faster and denser, electrical

	interconnects (wires) have begun to limit the performance of the systems that depends on them. In order to alleviate this problem, optical interconnects are being considered as an alternative. Some of the benefits of optical interconnects include higher speeds of operation with low drive requirements and minimal power dissipation, reduced size weight and cost, freedom from electromagnetic interference, crosstalk and ease of layout and routing. In order to implement optical interconnects, optoelectronic integrated circuits (OEICs) which integrate both electrical devices (transistors) with optical devices (optical detectors and emitters) must be created using electronic integrated circuits. However, due to intrinsic structure of silicon, this material is not capable of emitting light efficiently. Compound semiconductors such as GaAs on the other hand can be used to make LEDs and Lasers. Efforts are on without much success to develop technology that would support the monolithic integration of these two types of semiconductors. Therefore, it is proposed to develop a new technology which can combine silicon and GaAs substrates by wafer bonding or Epitaxy on Elec tonics (EoE).
B.15	**Modelling of buried channel MOSFET:** The existing CCD process development at SCL is based on buried channel technology to cater the need of high Charge Transfer Efficiency with high SNR. The output stage of CCD comprises of multiple stage source follower amplifier connected with sense node to produce voltage equivalent of collected charge with greater sensitivity. To design CCD output amplifier, modeling of n-buried channel MOSFET is required using SPICE.