B	Area	Process Technology (SCL)
B1	Sub Area	CMOS Process (SCL)
B1.1	**Design/PDK enablement of new devices in SCL's 180nm CMOS process** Software files need to be developed for various IC design elements while working with EDA tools. Following IC design elements are part of PDK library: Device symbols, CDF parameters, SKILL codes, Layout programmable cells (PCELLs), DRC, LVS, PEX verification rule decks. Software files need to be developed for these design elements for any device which needs to be integrated inside IC design flow. Skill set required for this work is good knowledge of EDA software programming along with background knowledge in semiconductor and IC domain	
B1.2	**Technology Development of High Power RF LDMOS Device** SCL has initiated in-house development of high Power RF LDMOS devices. In this work development of two different RF LDMOS devices for 650MHz (~500Watt) and 325MHz (1kWatt) operations has been initially targeted. In this regard SCL requires support for following topics: 1. Device Design for state of the art and reliable, rugged High voltage (~50V) RFLDMOS. 2. Process & Implant conditions (must be supported with TCAD simulated results). 3. Test chip for RF LDMOS process integration 4. RF characterization and Reliability analysis of developed devices.	
B1.3	**Enablement of dual supply (1.8V/3.3V) PDSOI CMOS process at 180nm node** SCL has achieved operational 1.8V PDSOI MOSFETs in 180nm technology. SCL is looking forward to next level of performance optimization. This should be demonstrated with - design of test chip comprising of structures required for SPICE model generation - test circuits like ring oscillator, registers, SRAM, etc. for dc/ac/radiation performance evaluation	

	- scalable SPICE model applicable to range of voltage, temperature (-55C to 125C) and frequency - I/O pads - test structures for reliability assessment to be part of test chip - test structures for RF performance evaluation
B1.4	**Modeling of High Voltage (10-20, 40-60V) N /P LDMOS devices developed at SCL in 180nm CMOS baseline process technology** A Simple concise statement about the investigation/theme and the expected deliverables in around 250 words Process development work at SCL is in progress for the process integration of LDMOS (VDS: 10-20, 40-60V; VGS: 3.3-5V) devices (n and PMOS) in standard 180nm baseline process. Once the devices are enabled, SPICE device models are required for the above LDMOS devices for circuit design implementation. The developed models should be accurately predicting both DC and AC performance of the devices over a range of voltage, temperatures (-55 to 125C) and frequencies.
B2	**Sub Area** | **CCD Process (SCL)**
B2.1	**Modelling of buried channel MOSFET:** The existing CCD process development at SCL is based on buried channel technology to cater the need of high Charge Transfer Efficiency with high SNR. The output stage of CCD comprises of multiple stage source follower amplifier connected with sense node to produce voltage equivalent of collected charge with greater sensitivity. To design CCD output amplifier, modelling of n-buried channel MOSFET is required using SPICE.