A. Research Areas in VLSI Design

A.1	**Design of instrumentation amplifier** The brief specifications are: Programmable Gain: 1 to 1000 Low noise:0.3μV p-p at 0.1 Hz to 10 Hz Low nonlinearity 0.01%(Gain = 1) High CMRR (Common Mode Rejection Ratio): 90dB (Gain=1) Low offset voltage: 100μV 3 dB Bandwidth: 1MHz (at Gain = 1)
A.2	**Design of a current feedback amplifier** The brief specifications are: High speed: 1650 MHz (G = +1) Low voltage offset: 0.7 mV Low input bias current: 7μA High O/p drive : 100 mA
A.3	**Design of low Noise amplifier** The brief specifications are; To operate from 1.8V power supply To give flat gain from 3 to 5 GHz To deliver 21 dB power gain with only -15dB variation Average noise figure to be 5.4 dB Input and output reflection coefficients to be -13.3 and -19.5 dB
A.4	**Design of DAC 12bit, 1Gbps, power(<250mW), low offset 3.3V supply,0.18um SCL technology**
A.5	**Design of DAC 14 bit, 500Mbps, power (<450mW), low offset, 3.3V supply,0.18um SCL technology**

A.6	**Design of Programmable Gain Amplifier PSRR>94dB, CMRR>80dB, Gain range 0.1 to 100, Gain Error :0.1%,Gain Drift :5ppm/^{o}C**
A.7	**Design of 8 bit, 500 MHz, low power(<100mW), Low offset Flash ADC, 3.3V supply,0.18um SCL technology**
A.8	**Design of Low offset (75µVMax) and low drift 1.3µV/^{o}C OPAMP**
A.9	**Design of PLL with VCO, 25MHz -3000MHz,Ultra low phase noise -110dBc/Hz, very low RMS jitter<180fs**
A.10	**Design of adjustable high performance Rad hard negative voltage regulator, Input supply ranges from - 3 V to - 12 V,3 A low dropout voltage**
A.11	**Design of Controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard, capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.**
A.12	**Design of ultra-low-noise, high-precision voltage reference** **< 1 ppm/°C Drift with 1.8V VDD** Supply Variation = ± 10 % ; Temp. Range = -40 deg C to +125 deg C
A.13	**Design of ultra-low-noise, high-precision voltage reference (1.2V) < 5ppm/°C Drift with 3.3V VDD** Supply Variation = ± 10 % ; Temp. Range = -40 deg C to +125 deg C
A.14	**Design of Radiation Hardened Dual port SRAM – different cuts**
A.15	**Forward Error Correction (FEC) multi bit Memory error correction techniques in Radiation environment**
A.16	**Development of Memory Compiler (Radhard) for SP and DP SRAM – to generate all views like .db., .lib, .v, .sdfetc**
A.17	**Design of High Speed CMOS Standard Cell Library in 0.18um SCL process :** The Standard Cell library should fullfill the following criteria : 1. Static CMOS Library 2. PVT variation : not more than 20% 3. D flip-flops in the library should be working up to 2GHz clock frequency 4. Library should have Multibit D Flip-flops : 2bits, 4 bits, 8bits

	5. Tracks : 9 or 12 (any one for complete library) 6. Supply Voltage 1.8V 7. Temperature range -40 to 125 C 8. Views and files required in the library
A.18	**Design of Low Power CMOS Standard Cell Library in 0.18um SCL process :** The Standard Cell library should fullfill the following criteria : 1. Static CMOS Library 2. PVT variation : not more than 20% 3. Library should have Multibit D Flip-flops : 2bits, 4 bits, 8bits 4. Power gating and Clock gating cells should be there 5. Tracks : 9 or 12 (any one for complete library) 6. Supply Voltage : 1.2V 7. Temperature range -40 to 125 C 8. Views and files required in the library
A.19	**High Voltage Difference Amplifier** Brief Specifications: 1) Programmable Gain = 0.05, 0.1, 0.4, 1 2) CMRR > 90dB 3) PSRR > 80 dB 4) 3 dB Bandwidth > 1MHz (at Gain = 1) 5) Non-linearity < 0.01% (at Gain = 1)
A.20	**Design of DSP Processor (180nm)**
A.21	**Design of Memory controller and other microprocessor peripherals**
A.22	**Design of USB 3.0 OR HIGHER**
A.23	**Design of Radiation Hardened Analog MUX 2:1, 4:1 and 8:1**
A.24	**Design of Radiation Hardened Flip-Flops**