Semi-Conductor Laboratory

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Corrigendum-I

Name: - Augmentation & Enhancement of Existing 8-inch Fab of Semi-Conductor Laboratory (SCL), India

CPPP Portal E-Tender ID: CPPP 2025_SCL_849478_1

It is to inform all prospective bidders/PSUs that the following corrigendum for the above-mentioned work has been provided as detailed below.

Page no./ section	sub section	Present statement	To be read as
Page 27/ section 1.5.2 Bid Package 2	B. Scope of Technology Transfers, Point 2 ©	LDMOS / DEMOS devices suitable for different voltage ranges (up to 10, 15, 20, 40V) and BJTs	LDMOS / DEMOS devices suitable for different voltage ranges (|Vds| up to 10, 15, 20, 40V) and BJTs
Page 116/ section 1.23 (Appendix:13)	Detailed Scope of Work for RFCMOS point no. 9	9. Contractor(s) shall perform models tuning & qualification to reliability verification and update the SCL PDK as per the optimized performance in SCL process	9. Contractor(s) shall perform device models tuning & model validation and update the SCL PDK as per the optimized performance in SCL process
Page 119/ section 1.23 (Appendix:14)	Detailed Scope of Work for BCD (HV LDMOS) Technology point no. 14 (a)	LDMOS & DEMOS Devices i) Medium Voltage scalable N&P LDMOS (|Vgs|=1.8 & 5V, |Vds|=7-15V) ii) High Voltage scalable N&P LDMOS (|Vgs|=1.8 & 5V, |Vds|=15-40V) iii) Scalable N&P DEMOS (|Vgs|=5V, |Vds|=up to 40V)	LDMOS or DEMOS Devices i) Medium Voltage scalable N-channel & P-channel LDMOS/DEMOS (|Vgs| of 3.3V or 5V, |Vds|=7-15V) ii) High Voltage scalable N-channel & P-channel LDMOS/DEMOS (|Vgs| of 3.3V or 5V, |Vds|=15-40V) iii) Scalable N-channel & P-channel DEMOS (|Vgs|=3.3V or 5V, |Vds| up to 40V) All the above mentioned high-voltage LDMOS/DEMOS devices should be integrated in 1.8V/3.3V or 1.8V/5V baseline CMOS process.
Page 28/Section 1.5.2	B. Scope of Technology Transfers/ Point 3c	Table 5: CMOS Image Sensor Pixel Specifications Parametr: Photodiode type PPD (Pinned Photo Diode) Value: Pinned	Table 5: CMOS Image Sensor Pixel Specifications Parameter: Photodiode type PPD (Pinned Photo Diode) Value: Pinned Photodiode (PPD)

		Photodiode (PPD) and Deep Depletion Extension (DDE)	
Page 121/ Appendix 15: Detailed Scope of Work for CIS Technology in SCL 180nm CMOS Process	Point 1	1) The technology provider shall demonstrate a completely functional 1Kx1K CIS detector with global shutter operation in SCL 180nm fab meeting the performance parameters as under: a) Support pixel sizes ranging from 5 to 40 micron in 3.3V b) Compatible with front side and backside illumination c) Pinned photo-diode (PPD) with <1% image lag d) Fully depleted thick substrate for Near IR for soft Xray sensitivity and global shutter operation e) Enhanced sensitivity in NIR region (> 70% QE for wavelengths above 800nm)	1) The technology provider shall demonstrate a completely functional 10µm pixel, 1Kx1K CIS imager with global shutter operation in SCL 180nm fab meeting the performance parameters as under: a) Compatible with front side and backside illumination b) Pinned photo-diode (PPD) with <1% image lag c) Enhanced sensitivity in NIR region (> 65% QE at wavelength 800nm)
Page 121/ Appendix 15: Detailed Scope of Work for CIS Technology in SCL 180nm CMOS Process	Point 3	3) Contractor(s) should demonstrate functionality stated in point no. 2 above along with target parameters stated in point no. 1)(f) above preferably with pixel sizes of at least 5µm, 10µm and 40µm in array size of at least 5 x 5.	3) Contractor(s) should demonstrate functionality stated in point no. 2 above along with target parameters stated in point no. 1)(f) above with pixel sizes of at least 5µm, 10µm and 40µm in array size of at least 5 x 5.

Note: - Based on the requests received from prospective vendors, the bid query submission deadline has been extended until 24/03/2025 at 11:00 AM (IST). All prospective vendors are requested to submit their queries by the given date and time to the email address fab_pm@scl.gov.in. No further queries will be entertained.