Semi-Conductor Laboratory
S.A.S. Nagar

Record of clarifications provided to the queries of the prospective bidders during the Pre-bid Conference held at SCL on February 06, 2018 in response to Public Tender Notice No. SCL/PT/107 (Tender No. SCL/PS2/2017E0089301) for Memory Compiler Radhard Single Port SRAM Compiler.

A. Vendor Name: M/s CoreEl Technologies, Bangalore

Q1: Is this tender for readymade product or vendor can develop the solution and then delivery

SCL Response: It is a customized software/EDA tool dedicated for SCL's 180 nm process. Vendor has to make test chip(s), software and demonstrate the results on Silicon after few (if any) iterations. However experience in this field for other foundries will definitely help them.

Q2: What will be delivery period for this (12 months is mentioned in the document – can it be extended?)

SCL Response: Delivery period is restricted to 12 months only, it can only be extended in case there is delay in fabrication, packaging, testing at SCL end. Various milestones mentioned in **Annexure 3 (Work Activity Flow between SCL and Vendor)** needs to be achieved in time, such that whole product should be delivered in 12 months.

Q3: Re Confirm the GST – 5%

SCL Response: Purchaser is entitled to concessional IGST of 5 % as per Ministry of Finance, Department of Revenue, Notification No. 47/2017 Integrated Tax (Rate) dated 14th November, 2017 and would accordingly issue Exemption Certificate in favour of the contractor quoting in Indian Rupees.

B. Vendor Name: M/s Cadre Design Systems, Delhi on behalf of M/s Cogenda Pte Ltd, Singapore

Q1: Regarding section 1, item 1.19, please clarify if extra pin is allowed to indicate the power-down mode.

SCL Response: Extra pin will be required only if power down option is enabled while generating the memory cut, otherwise no extra pin should be there.

Q2: Regarding section 1, item 1.23, please clarify that byte-enable and bit-enable features are for separate memory cut. In another word, it is NOT expect that a single memory cut has bit-enable and byte-enable at the same time.

SCL Response: Yes both features are not meant for single memory cut. Single cut will be having single feature (either bit-enable or byte-enable).

Q3: Regarding section 1, item 1.27, please clarify if schematics can be provided in drawings, instead of in Cadence Virtuoso format. The vendor does not use Cadence Virtuoso in its design flow, so schematics are only available in drawing. On the other hand, netlist will be provided in industrial-standard SPICE format.

SCL Response: Schematic in cadence environment is preferred. Otherwise schematic in PDF/PNG of each block, sub-block of generated memory cut is required upto MOSFET level.

Q4: Regarding section 1, item 1.31, please clarify that SEU rate of 10e-10 upset/bit-day is the rate after EDAC correction is applied.

SCL Response: This radiation level is after EDAC correction logic.

Q5: Regarding section 1, item 3.3, SRAM compiler applies pessimism in timing estimation to ensure the generated memory meets the timing constraints in all conditions. Therefore, the simulated characteristics is going to be better than specifications. Please clarify that simulation being better than specification does not violate the 5% tolerance criteria.

SCL Response: Yeah 5% is the maximum allowed deviation. Anything less than this deviation will always be welcome.

C. Vendor Name: M/s Album Semiconductors (I) Pvt. Limited, Bangalore

Q1: What is the calendar start date and end date of the project ?

SCL Response: Start date will be the date of P.O., after which PDK will be given to the vendor after NDA signature and delivery date will be 12 months from date of P.O.

D. Vendor Name: M/s Synopsys International Limited, Ireland/Bangalore

Q1: Whether RH-Bitcell will be provided by SCL or not ?

SCL Response: No, RH-Bitcell is not provided by SCL. Vendor has to build his own radiation hardened bit cell along with all radiation hardened periphery. Vendor can use Non-RH bitcell of SCL 's PDK and apply radiation hardening techniques to it and provide SCL the RH memories.

E. Vendor Name: M/s Zia Semiconductor Pvt Ltd, Bangalore

No Queries

General Comment:

1. Vendors expressed satisfaction on the response/clarifications provided to their queries.

2. The prospective bidders must take the responses / clarifications as recorded herein into account while submitting the bid to SCL.

Sr. Purchase & Stores Officer